Elektor Electronics

September 1987

Horn loading revisited

Stream encryption

EPROM emulator

UK £1.30
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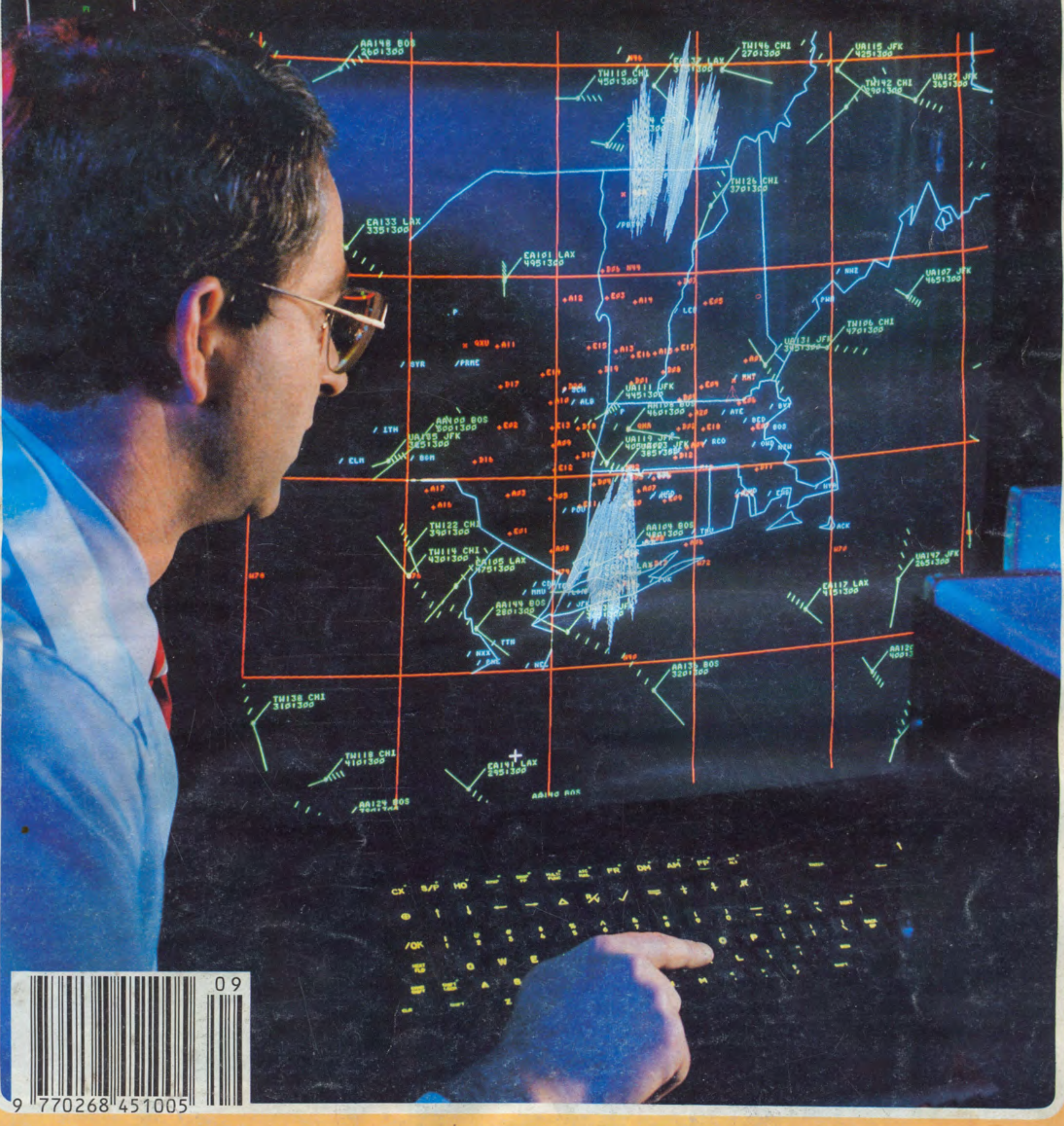
SINGLE-CHIP MICROCONTROLLERS



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Elektor Electronics

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Front cover
A new colour-coded air-traffic control system designed to simplify aircraft identification and improve clarity is being evaluated in the United States by the Federal Aviation Administration (FAA). The new Hughes-Sanders Advanced Automation System (AAS) incorporates display consoles that make greater use of colour to distinghuish aircraft movements and other data. The visual display is in four colours: aircraft tracks are shown in green; city and state boundaries in light blue; extreme weather conditions in white; and other data in red. Shown here, a Hughes Aircraft Company engineer tests the colour and brightness of the console display with the aid of simulated aircraft tracks over New England.

A difficult trading year

In its annual report for 1986, the Electronic Engineering Association says that sales by its members during the year exceeded £24 billion, of which half is the supply of equipment and half is now the provision of systems and services (augmented by British Telecom). This is a significant trend in the development of the UK electronics industry in a deregulated environment, and it is expected that sales of equipment will grow more slowly than the provision of systems and services.

Total sales of components and equipment in 1986 was marginally lower than 1985 (Fig. 1). The reduction was due to a 9% reduction in exports principally in the data processing sector (Fig. 2). Sales and exports of radio and electronic capital goods grew, with strong performances in radar, navigational aids and simulators. Sales and exports in the sub-assembly and components sector equalled 1985.

As expected from the overall static sales figures, the production index fell 5% in 1986, after a strong 14% annual growth between 1980 and 1985 (Fig. 3). Production of components and communications equipment grew, balanced by falls in the data-processing and capital goods sector. This reflected the reduction in exports of data-processing equipment in a period of a strong pound and sluggish demand.

Exports are now over half of total equipment sales, although they include some re-exports of imported goods, particularly components. They are however exceeded in all sectors except capital goods by imports, indicating the extent to which overseas data processing equipment and components have continued to be purchased by UK users.

Research and Development in the electronics industry continues at a high level, at one-third of the total R&D in industry, but has turned down in real terms since 1983, after considerable growth in 1975 to 1981. Aerospace and mechanical engineering R&D expenditures are shown for comparison.

The decline of electronics R&D in 1983/85 may have influenced the non-growth of 1986 sales.

Production output trends throughout 1986 have been upwards in all sectors except radio and electronic capital goods, with particularly strong performances in the fourth quarter.

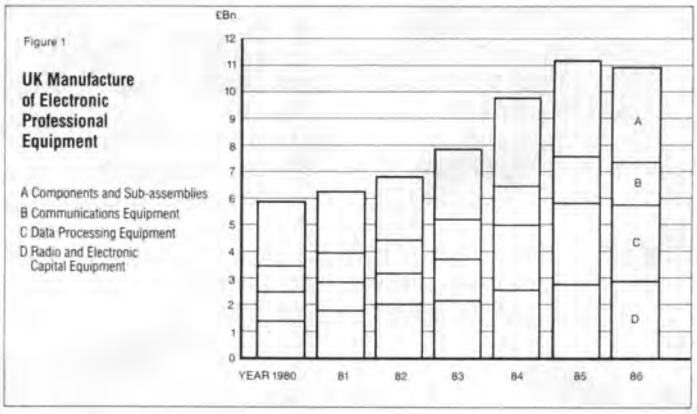


Figure 1
UK Manufacture of Electronic Professional Equipment

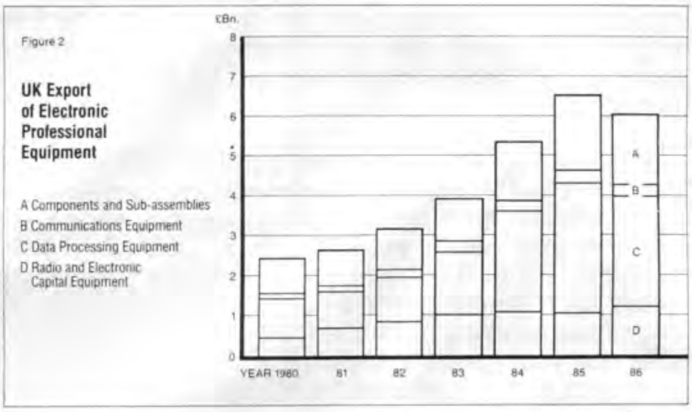


Figure 2
UK Export of Electronic Professional Equipment

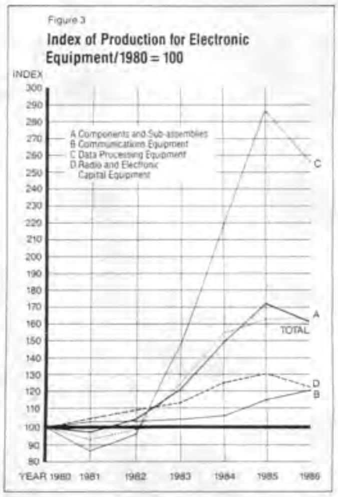


Figure 3
Index of Production for Electronic Equipment/1980 = 100

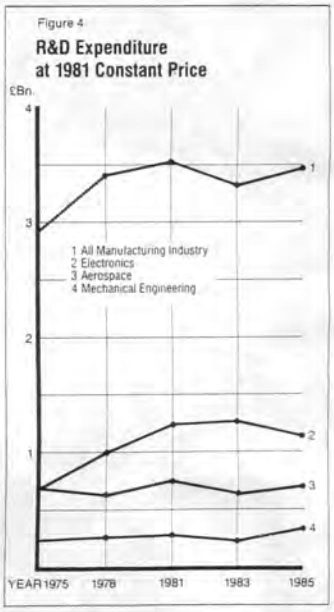


Figure 4
R&D Expenditure at 1981 Constant Price

Fibre optics for separating PCs from their printers

It is now possible to have personal computers located completely independently of their printers (or other peripherals) by using optical fibre cable. Not only does this eliminate the risks of electrical interference and static electricity, but it also overcomes the limit of about seven metres for parallel interfacing. The increase in separation distance can also contribute to the avoidance of noise and dust problems often associated with printers.

Fiberdata of Stockholm, Sweden, have developed fibre optic parallel interfaces to the Centronics and Data Products standards. This new technique enables data transfer over distances of up to four kilometres. The transfer rate can be as much as 15,000 lines of text per minute, equivalent to about 180 size A4 pages. This also means that it is possible for several computers to share a printer. Furthermore, the technique obviates any risk of eavesdropping or tapping into the connexion by outsiders.

Further information is available from **Brian Skelton • Tekelec Components Ltd • Cumberland House • Baxter Avenue • Southend-on-Sea SS2 6FA • Telephone (0702) 349419.**

ELECTRONICS NEWS • ELECTRONICS NI

Waltons, of 55a Worcester Street, Wolverhampton, a retail electronics outlet owned by the Dennes family since 1947, has been acquired by Marco Trading of Wem, Shropshire. Marco, established since 1972, already have a retail outlet in Wem, but are perhaps better known for their mail order business, which has an illustrated catalogue of over 100 pages covering some 6,000 lines. They also have a wholesale division offering a service to manufacturers, and an export/import section with worldwide contacts. The photograph shows Mr Jack Dennes (left), retiring proprietor, and Mr Martin Cox, a director of Marco.

PLESSEY LIFTS THE HEAT FOR SUPERCONDUCTIVITY

An end to risk-laden high-voltage electricity cables and pylons, and to the seizing up of mechanical bearings are among the benefits possible from experiments being carried out into superconductivity by Plessey.

Professor William Gosling, technical director of the Plessey Electronics & Communications Group, also predicts faster computers using less power from this ability of materials to lose their electrical resistance when kept at very low temperatures.

Until recently, it was thought that superconductivity was only possible at a temperature just a little above 0 K (absolute zero), which is the lowest possible for all substances, and maintaining such a condition is expensive.

Plessey has, however, demonstrated that superconductivity is possible at 191 K, a temperature that can be maintained in liquid nitrogen, a plentiful and relatively inexpensive commodity: in Britain it costs about the same as milk.

Engineers at Plessey's research laboratory at Caswell in the Midlands have shown that an electric current can be passed down cables for indefinite distances with no power loss at all. The key to this ability is in the development of ferroelectric ceramics which, though normally electrical insulators, are paradoxically conductive at low temperatures.

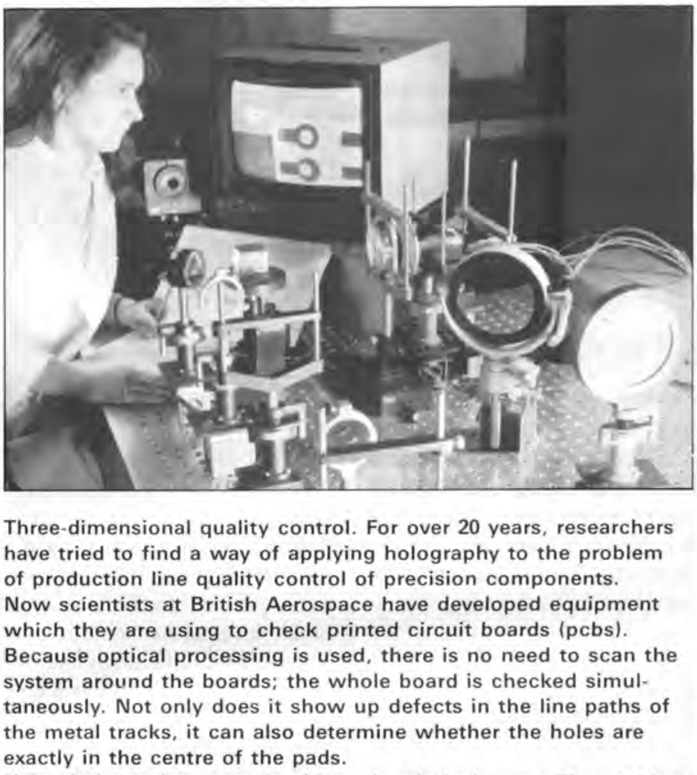
The superconductivity of these materials led Plessey, which has worked with ceramics for over 30 years, to establish a new research programme at Caswell this year.

Professor Gosling believes that in the electronics industry superconductivity could revolutionize radio communications and have a major effect on the design of radar equipment and of memory and logic circuits used in computers. He forecasts that IC's for computers based on superconductivity will be in experimental production within 18 to 24 months. (LPS)

Litton purchases solid-state microwave operation from Harris

Litton Industries of Zurich have acquired the solid-state microwave amplifier operation of Harris Corporation, shortly after purchasing the Microwave Products Division of Gould Inc.

Litton says that the aim of these acquisitions is to broaden its capabilities in solid-state microwave technology and to augment its products for electronic warfare and radar markets.



Three-dimensional quality control. For over 20 years, researchers have tried to find a way of applying holography to the problem of production line quality control of precision components.

Now scientists at British Aerospace have developed equipment which they are using to check printed circuit boards (pcbs). Because optical processing is used, there is no need to scan the system around the boards; the whole board is checked simultaneously. Not only does it show up defects in the line paths of the metal tracks, it can also determine whether the holes are exactly in the centre of the pads.

Using holography on static objects is relatively easy. The problem is to do it when there is vibration and in a factory environment, where equipment must be robust.

The company has overcome these problems by developing a new type of device called a spatial light modulator (SLM) which has the capability of converting ordinary light to the type for making laser holograms. This special light valve is the key ingredient and has been developed by the company so that its cost has been reduced tenfold compared with earlier version.

The optical Fourier Transform of the object under scrutiny is compared with a test hologram by a device incorporating the SLM and AESOP, short for Automatic Equipment of Surveillance using Optical Processing. Comparison of the two hologram images allows faults in the object under test to be located.

More important, perhaps, in the long term are the possible applications in the field of three-dimensional computer aided design (CAD). Some of the techniques involved could also have applications for three-dimensional television.

The picture shows tests on the AESOP system with an image of part of the pcb on the TV monitor. The device is not yet in commercial production, but further information can be obtained from British Aerospace PLC • Public Relations Department • PO Box 5 • Filton • BRISTOL BS12 7QW • England.

CROWN COPYRIGHT RESERVED

Cirkit, the Portsmouth and Broxbourne based distributor, has recently signed an agreement to handle the IDC connector system from Harwin. Pictured after signing the agreement are from left to right: Martin Greenslade, Distribution Manager, Harwin Engineers SA; Nick Hodge, Product Manager, Cirkit Distribution; Richard Bulgin, Chief Executive, Cirkit Holdings PLC; and Ken Hollingsworth, General Manager, Cirkit Distribution, Portsmouth.

SEMI to sponsor first SEMICON trade show in China

The Semiconductor Equipment and Materials Institute is to sponsor its first SEMICON trade show in Shanghai on 3-8 April, 1988. SEMICON shows are dedicated exclusively to exhibits of advanced technologies used in manufacturing semiconductor chips.

The addition of SEMICON/Shanghai brings the total number of SEMICON trade shows around the world to eight: three in the USA, two in Japan, one in Europe, one in Korea, and now one in China.

The new trade show is expected to attract some 50,000 people, including government and industry representatives from Beijing, Shanghai, Tianjin, and surrounding electronics centres.

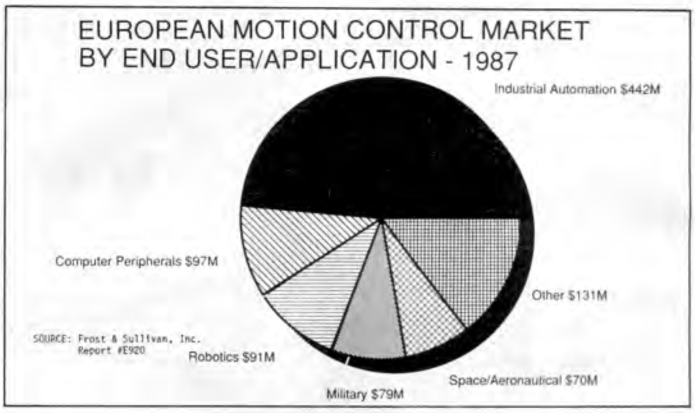
SEMI, the sponsor of SEMICON trade shows, is an international trade association for companies that supply semiconductor equipment and materials. SEMI serves more than 1,100 member companies in 18 countries around the world from its headquarters in Mountain View, California, and offices in London, Tokyo, and Washington D. C.

European motion control market

Spending on robots in Europe will rise nearly 20% a year through 1991, according to *Advanced Motion Controls in Europe* (#E920), a 348-page analysis recently completed by Frost & Sullivan.

Robotics is the fastest growing use of advanced motion controls—part of an $800 million high-tech arena set to double in Europe over the next five years. But even Federal Germany—Europe's largest user of robots—is far behind Japan, and it is doubtful whether this gap will ever be closed. None the less, robotics as an end use will climb from less than a tenth of all spending on advanced motion controls to about 12% by 1991.

The analysis cites the UK as a "notable exception" to the growth in robotics: the total number of robots in the UK in early 1986 was about 3,200—less than the **increase** in Federal Germany in 1985. The report ties the weakness of the UK industry to the fact that firms "are simply not automating nearly as fast" as their counterparts elsewhere, partly because high interest rates have inhibited investment. In 1986, Federal Germany accounted for 38% of all European spending on robots; France represented 16%; and the UK 14%.


EUROPEAN MOTION CONTROL MARKET BY END USER/APPLICATION - 1987

SOURCE: Frost & Sullivan, Inc.
Report #E920

Overall, advanced motion controls will grow more slowly than its robotics segment, although, at nearly 15% a year, the gains will be significant, since price drops have widened the affordability of the products. With applications that reach all the way into space, the report predicts the total European market will rise form $799 million in 1986 to $910 million in 1986, and $1.6 billion by 1991 (constant 1985 dollars).

200 Mbyte optical memory card

Optical Recording Corporation—ORC—of Toronto have entered a technology marketing agreement with LifeCard International of Townson, Maryland, a subsidiary of Blue Cross/Blue Shield.

ORC is in the business of developing prototype optical card drives and media for digital optical storage applications and the licensing of this technology to electronics and media manufacturers worldwide.

The optical card of credit card size will carry 50 to 200 Mbytes of user application data on one side, and the card drive is designed for a data transfer rate of over 1 Mbit/s in both the read and write functions.

This represents capacity and performance 100 times greater than that of Drexler Technology Corporation's Lasercard, and over 1,000 times that of the microchip-embedded Smart Cards.

Godiva boards for electronics education

The Education Division of Cirkit has acquired exclusive rights to distribute the Godiva range of modular printed-circuit boards for use in primary and secondary schools in CDT, Science, Maths, and Computer Studies.

The boards have been designed, developed, and tested by Coventry Education Authority Microelectronics Centre over a period of four years, during which time they have been used extensively within the Coventry TVEI programme.

The principle of Godiva boards is to promote a systems approach to electronics, encouraging students to analyse, investigate, and develop solutions to electronic control problems. Each module performs a single electronic function and, although some are more complex than others, each has a specific purpose corresponding to one of the basic circuit blocks used in electronic systems today. Through understanding each function, a novice can construct complex electronic systems without the need to understand the circuit theory in detail.

The range comprises 24 difference function boards, providing as many different circuit functions, which vary from simple logic gates up to a Z80 control board with 16 pre-programmed functions. Other modules to be introduced in the future will be an analogue-to-digital converter, EPROM programmer, stepper motor driver, and dual liquid crystal display.

Seen in the photograph are from left to right: Christopher Farmer, Director of Coventry Education Authority; Paul Gardiner, Director of Coventry Microelectronics Centre; and Mike Sandham, Sales Director of Cirkit Distribution Ltd.

The search for superconductors

Superconductivity is a phenomenon that occurs in many materials, particularly metals and alloys. When such materials are cooled to below a certain temperature (the transition temperature), their electrical resistance becomes negligibly small.

Also, when a conducting loop, in a weak magnetic field, is cooled to below the transition temperature, the magnetic flux becomes trapped in the loop. This is the so-called Meissner effect. The flux is sustained by supercurrents circulating around the loop. Any field variation is countered, by Lenz's Law, by the induction of an appropriate supercurrent.

An explanation of superconductivity was not available until 1957, when American scientists John Bardeen, Leon N. Cooper, and John R. Schrieffer published their theoretical work, now known as the BSC Theory.

Until recently, it was assumed that the transition temperature for all materials lay below 4 K. This temperature was established by the Dutch physicist and Nobel Prize winner, Heike Kamerlingh Onnes. Since it is costly and, outside a laboratory, impractical to achieve such low temperatures, nobody considered or envisaged any practical uses of superconductivity.

Within the past year, however, American scientists have produced ferroceramics that exhibit superconductivity at much higher temperatures—around 93 K. This has important consequences, because these temperatures lie above the transition temperature of nitrogen (77 K), which is a plentiful and very inexpensive element. In other words, ferroceramics can be made superconductive at temperatures that can be economically and practically be attainted.

Researchers are convinced that materials will soon be found or produced which will superconduct at room temperatures. When these arrive, they will herald an electro-technical revolution.

Until then, scientists the world over will search feverishly for these new materials. To that end, some of the UK's foremost electronics companies will formulate a strategy for research in this fascinating (and rewarding) technology. Already, a steering committee for representatives of a number of these companies has been set up by the Department of Trade and Industry.

Funding for the programme, which will run into many millions of pounds, is expected to be borne by the electronics industry, the Department of Trade and Industry and the Science and Engineering Research Council.

At the same time, the European Commission is also setting up a number of initiatives into research on superconducting materials under existing European research and development programmes, such as European Action for Magnets (EURAM), and Stimulating Action, which is a general programme for original research.

Electronic Brokers has recently signed an agreement with Lloyd Instruments PLC to distribute selected products from the company's range of British-made chart recorders and plotters, including the recently introduced Graphic 1000 and 2000 recorders and the PL3 low-cost A3 plotter. Seen in the photograph after the signing of the agreement are from left to right: Peter Jackson, Area Sales Manager of Lloyd Instruments, and Julian Shaw, Head of Electronic Brokers' Test & Measurement Division.

SINGLE-CHIP MICROCONTROLLERS

Single-chip microcontrollers, such as Intel's MCS-51 series described in this article, are currently finding their way in more and more industrial control systems. They offer a remarkably low chip-count as well as ease of programming when the computer is assigned a single task.

For many applications, the use of a dedicated microcontroller has obvious advantages over a standard microprocessor like the 6502 or Z80. This is mainly due to the microcontroller being tailored to perform only the necessary functions. Input/output lines, for instance, are available direct on the chip, obviating the need for a complex set-up with individual I/O chips, interfaces, buffers, and all the necessary hardware for address and data decoding. Often, the microcontroller holds a programmable timer/counter also, and has an extensive instruction set for bit manipulation.

The Types 8051 and 8052 are single-chip microcontrollers from Intel's extensive MCS-51 series. Over the past years, they have found an increasing number of applications in industrial processing systems. This introduction aims at familiarizing you with the 8051, 8052 and 8052AH-BASIC, which are versatile and powerful controllers that enable designing and building compact, microprocessor-based, equipment for a wide range of applications.

MCS-51 Microcontrollers.

Technical features:

- 8-bit CPU optimized for control applications.
- Extensive Boolean processing (single-bit logic).
- 32 bidirectional and individually addressable I/O lines.
- 128 or 256 bytes of on-chip data RAM.
- 2 or 3 16-bit timer/counters.
- Programmable, full duplex UART.
- 5 or 6-source interrupt structure with 2 priority levels.
- On-chip clock oscillator.
- 4 or 8 Kbytes of on-chip program memory (8751 & 8752: EPROM).
- 64 Kbyte program memory address space.
- 64 Kbyte data memory address space.
- 111 instructions (64 single-cycle).
- Decimal and hexadecimal operations.
- 8 Kbyte BASIC interpreter (8052AH-BASIC).
- Built-in EPROM programmer under BASIC control (8052AH-BASIC).
- Special BASIC commands for I/O, counters, and serial interface (8052AH-BASIC).

The MCS-51 family

Intel's MCS-51 family of single-chip microcontrollers consists of the devices listed in Table 1. It should be noted that the type indication 8051 often refers to the the MCS-51 family as a whole. The pinning and functional representation of some of the chips in the MCS-51 family appear in Fig. 1 and Fig. 2 respectively. The 8051 is a controller with 4 Kbytes of on-chip, mask programmable, ROM. The Type 8052AH, a HMOS II chip, is an an enhanced, downward compatible version of the 8051. It is important to note that the 8051, 8051AH and 8052AH are mask-programmable devices. This means they are only available in large quantities since the on-chip program memory can only be loaded by the manufacturer. The 8031, however, differs from the 8051 in not having the on-chip ROM. Instead, it fetches all instructions from external memory, and is, therefore, ideal for writing and testing software for the 8051. Similarly, the 8031AH and 8032AH are the ROM-less versions of the 8051AH and 8052AH, respectively, while the corresponding EPROM versions are identified as Types 8751 and 8752. Software security can be provided by making the EPROM contents inaccessible for external read devices. A separate product, the 8052AH-BASIC, is essentially a 8052AH with a powerful and fast BASIC interpreter programmed in the on-chip ROM. This microcontroller chip is particularly interesting for one-off applications, and will be reverted to in greater detail.

Memory organization

Essentials of the memory structure of chips in the MCS-51 series appear in Fig. 3. In brief, the memory is divided in 2 blocks of 64 Kbytes. One block is the program memory, the other the data memory. The lower 4 or 8 Kbytes of the

1

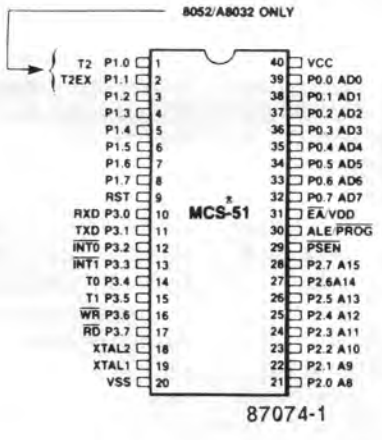


Fig. 1 Pin assignment for the chips in the MCS-51 series.

2

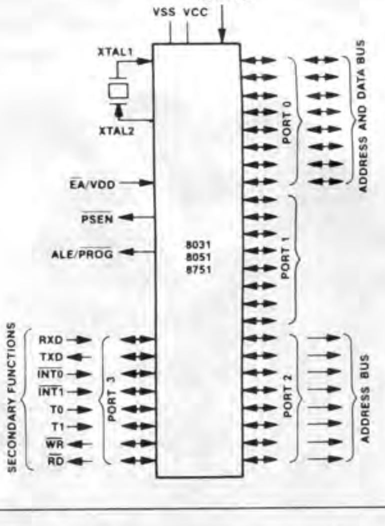


Fig. 2 Showing the port line functions when the controller operates with external memory.

Table 1

Device	Internal Memory		Timers/ Event Counters	Interrupts
	Program	Data		
8052AH	8K × 8 ROM	256 × 8 RAM	3 × 16-Bit	6
8051AH	4K × 8 ROM	128 × 8 RAM	2 × 16-Bit	5
8051	4K × 8 ROM	128 × 8 RAM	2 × 16-Bit	5
8032AH	none	256 × 8 RAM	3 × 16-Bit	6
8031AH	none	128 × 8 RAM	2 × 16-Bit	5
8031	none	128 × 8 RAM	2 × 16-Bit	5
8751H	4K × 8 EPROM	128 × 8 RAM	2 × 16-Bit	5
8751H-12	4K × 8 EPROM	128 × 8 RAM	2 × 16-Bit	5

Table 1 The MCS-51 family of microcontrollers.

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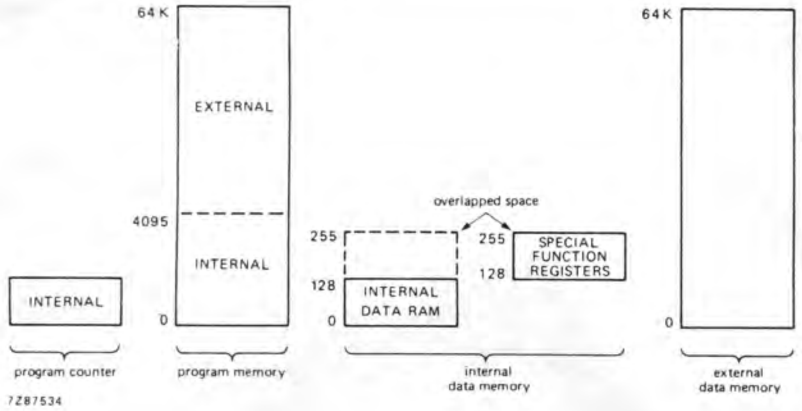

Fig. 3 The MCS-51 memory structure.

4

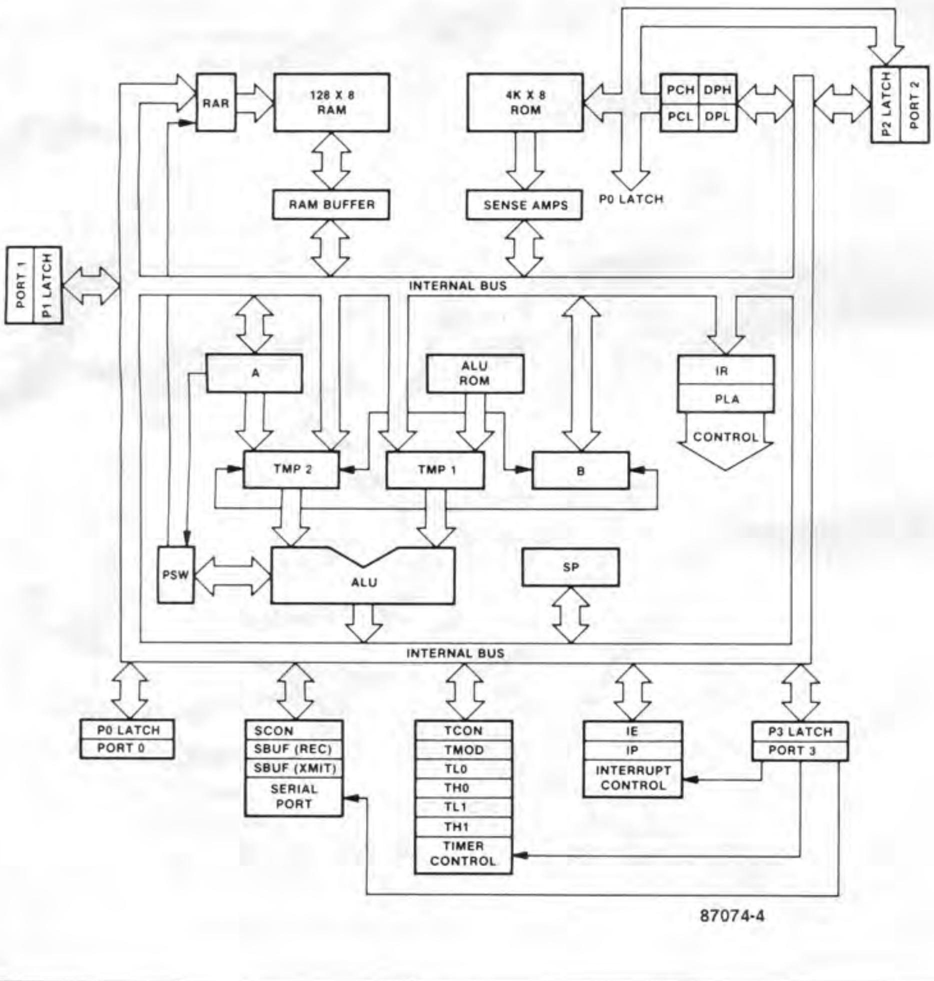

Fig. 4 The MCS-51 architecture.

program memory is on-chip ROM. In the ROM-less controllers, all program memory is external, and may, therefore, be RAM or (EP)ROM. The microcontrollers can only read from the program memory, which holds the sequence of executable processor instructions in the form of machine code. The data memory is used for storing variables, intermediate results of calculations, processed datawords, look-up tables, and the like. Up to 64 Kbytes of external ROM, RAM or EPROM can be addressed in the external data memory space. A number of special register functions are located in a separate 128 or 256 Byte RAM area. The main registers are the accumulator, register B (for multiplication and division), status register, stack pointer, data pointer (2×8 bits or 1×16 bits), port 0...3, the double serial transmit/receive register, the 16-bit timer/counter registers, capture registers for the third counter (8052), and the command registers for special functions (interrupts, RTC, serial I/O).

Most MCS-51 instructions are executed in a single machine cycle, i.e., within 12 clock periods. When the clock frequency is 12 MHz, one machine cycle lasts 1 μs, so that the processing speed of the MCS-51 chip equals that of a 6502 CPU running at 2 MHz, or a Z80 at 8 MHz. A noteworthy aspect of the microcontrollers is their ability to manipulate fewer than 8 bits at a time, relieving the programmer of cumbersome bit-masking routines.

Buses and ports

The basic internal structure of a controller in the MCS-51 family is shown in Fig. 4. It is seen that there are, in theory, 4 bidirectional, 8-bit wide ports. In practice, these are only available when the internal memory (ROM or RAM) is used. In all other cases, ports 0 and 2 function as the data and address bus (refer back to Fig. 2), so that 2 ports remain for I/O applications. Port P2 supplies address signals A15...A8, port P0 address signals A7...A0 and databits D7...D0, multiplexed with the aid of the ALE pulse (adress latch enable). Outputs $\overline{RD}$ and $\overline{WR}$ are simply output lines on port 3, internally programmed for supplying the pulses for read and write operations in the external data memory. The read strobe for external program memory is the signal $\overline{\text{PSEN}}$ (program store enable). It is interesting to note that $\overline{\text{PSEN}}$, as well as ALE, is activated twice in every machine cycle during execution of a program in (EP)ROM, because two bytes are fetched successively during each cycle. $\overline{\text{PSEN}}$ remains inactive when the machine code is stored in the internal memory, and the external memory (if available) is empty. $\overline{\text{PSEN}}$ is not normally used in designs incorporating the 8052AH-BASIC, because the internal ROM holds the BASIC interpreter. Input $\overline{\text{EA}}$ (external address) is activated when the processor is to read opcodes from the external memory, rather than from its internal (EP)ROM. The $\overline{\text{EA}}$ input is also used for applying the 21 V programming voltage for the internal EPROM (8751, 8752).

Timers and counters

It was already seen in Table 1 that the 8052 has one more 16-bit timer/counter than the 8051. Below is a necessarily concise overview of the functions performed by the timer/counter blocks.

In the timer mode, the register contents are incremented once in every machine cycle. The maximum count rate is therefore 1/12th of the processor clock speed. In the counter mode, the register contents are incremented on the trailing edge of the signal applied to input T0, T1, or T2 (the latter is only available on the 8052). The maximum count rate is 1/24th of the processor clock speed. Counter/timers 0 and 1 have 4 programmable modes, including 8 or 16 bit operation, and automatic loading of a preset value. Timer/counter 1 can be programmed to function as a baudrate generator for the asynchronous serial interface. Timer/counter 2 (8052 only) has 3 modes: 16-bit automatically reloadable counter, 16-bit capture counter, and baudrate generator.

The serial port

All microcontrollers in the MCS-51 family feature an on-chip, bidirectional serial inter-

Table 2

ARITHMETIC OPERATIONS

Mnemonic		Description	Byte	Cyc
ADD	A,Rn	Add register to Accumulator	1	1
ADD	A,direct	Add direct byte to Accumulator	2	1
ADD	A,@Ri	Add indirect RAM to Accumulator	1	1
ADD	A,#data	Add immediate data to Accumulator	2	1
ADDC	A,Rn	Add register to Accumulator with Carry	1	1
ADDC	A,direct	Add direct byte to A with Carry flag	2	1
ADDC	A,@Ri	Add indirect RAM to A with Carry flag	1	1
ADDC	A,#data	Add immediate data to A with Carry flag	2	1
SUBB	A,Rn	Subtract register from A with Borrow	1	1
SUBB	A,direct	Subtract direct byte from A with Borrow	2	1
SUBB	A,@Ri	Subtract indirect RAM from A w/ Borrow	1	1
SUBB	A,#data	Subtract immed. data from A w/ Borrow	2	1
INC	A	Increment Accumulator	1	1
INC	Rn	Increment register	1	1
INC	direct	Increment direct byte	2	1
INC	@Ri	Increment indirect RAM	1	1
DEC	A	Decrement Accumulator	1	1
DEC	Rn	Decrement register	1	1
DEC	direct	Decrement direct byte	2	1
DEC	@Ri	Decrement indirect RAM	1	1
INC	DPTR	Increment Data Pointer	1	2
MUL	AB	Multiply A & B	1	4
DIV	AB	Divide A by B	1	4
DA	A	Decimal Adjust Accumulator	1	1

LOGICAL OPERATIONS

Mnemonic		Destination	Byte	Cyc
ANL	A,Rn	AND register to Accumulator	1	1
ANL	A,direct	AND direct byte to Accumulator	2	1
ANL	A,@Ri	AND indirect RAM to Accumulator	1	1
ANL	A,#data	AND immediate data to Accumulator	2	1
ANL	direct,A	AND Accumulator to direct byte	2	1
ANL	direct,#data	AND immediate data to direct byte	3	2
ORL	A,Rn	OR register to Accumulator	1	1
ORL	A,direct	OR direct byte to Accumulator	2	1
ORL	A,@Ri	OR indirect RAM to Accumulator	1	1
ORL	A,#data	OR immediate data to Accumulator	2	1
ORL	direct,A	OR Accumulator to direct byte	2	1
ORL	direct,#data	OR immediate data to direct byte	3	2
XRL	A,Rn	Exclusive-OR register to Accumulator	1	1
XRL	A,direct	Exclusive-OR direct byte to Accumulator	2	1
XRL	A,@Ri	Exclusive-OR indirect RAM to A	1	1
XRL	A,#data	Exclusive-OR immediate data to A	2	1
XRL	direct,A	Exclusive-OR Accumulator to direct byte	2	1
XRL	direct,#data	Exclusive-OR immediate data to direct	3	2
CLR	A	Clear Accumulator	1	1
CPL	A	Complement Accumulator	1	1
RL	A	Rotate Accumulator Left	1	1
RLC	A	Rotate A Left through the Carry flag	1	1
RR	A	Rotate Accumulator Right	1	1
RRC	A	Rotate A Right through Carry flag	1	1
SWAP	A	Swap nibbles within the Accumulator	1	1

DATA TRANSFER

Mnemonic		Description	Byte	Cyc
MOV	A,Rn	Move register to Accumulator	1	1
MOV	A,direct	Move direct byte to Accumulator	2	1
MOV	A,@Ri	Move indirect RAM to Accumulator	1	1
MOV	A,#data	Move immediate data to Accumulator	2	1
MOV	Rn,A	Move Accumulator to register	1	1
MOV	Rn,direct	Move direct byte to register	2	2
MOV	Rn,#data	Move immediate data to register	2	1
MOV	direct,A	Move Accumulator to direct byte	2	1
MOV	direct,Rn	Move register to direct byte	2	2
MOV	direct,direct	Move direct byte to direct	3	2
MOV	direct,@Ri	Move indirect RAM to direct byte	2	2
MOV	direct,#data	Move immediate data to direct byte	3	2
MOV	@Ri,A	Move Accumulator to indirect RAM	1	1
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2
MOV	@Ri,#data	Move immediate data to indirect RAM	2	1
MOV	DPTR,#data16	Load Data Pointer with a 16-bit constant	3	2

DATA TRANSFER (cont.)

Mnemonic		Description	Byte	Cyc
MOVC	A,@A+DPTR	Move Code byte relative to DPTR to A	1	2
MOVC	A,@A+PC	Move Code byte relative to PC to A	1	2
MOVX	A,@Ri	Move External RAM (8-bit addr) to A	1	2
MOVX	A,@DPTR	Move External RAM (16-bit addr) to A	1	2
MOVX	@Ri,A	Move A to External RAM (8-bit addr)	1	2
MOVX	@DPTR,A	Move A to External RAM (16-bit addr)	1	2
PUSH	direct	Push direct byte onto stack	2	2
POP	direct	Pop direct byte from stack	2	2
XCH	A,Rn	Exchange register with Accumulator	1	1
XCH	A,direct	Exchange direct byte with Accumulator	2	1
XCH	A,@Ri	Exchange indirect RAM with A	1	1
XCHD	A,@Ri	Exchange low-order Digit ind. RAM w/A	1	1

BOOLEAN VARIABLE MANIPULATION

Mnemonic		Description	Byte	Cyc
CLR	C	Clear Carry flag	1	1
CLR	bit	Clear direct bit	2	1
SETB	C	Set Carry flag	1	1
SETB	bit	Set direct Bit	2	1
CPL	C	Complement Carry flag	1	1
CPL	bit	Complement direct bit	2	1
ANL	C,bit	AND direct bit to Carry flag	2	2
ANL	C,/bit	AND complement of direct bit to Carry	2	2
ORL	C,bit	OR direct bit to Carry flag	2	2
ORL	C,/bit	OR complement of direct bit to Carry	2	2
MOV	C,bit	Move direct bit to Carry flag	2	1
MOV	bit,C	Move Carry flag to direct bit	2	2

PROGRAM AND MACHINE CONTROL

Mnemonic		Description	Byte	Cyc
ACALL	addr11	Absolute Subroutine Call	2	2
LCALL	addr16	Long Subroutine Call	3	2
RET		Return from subroutine	1	2
RETI		Return from interrupt	1	2
AJMP	addr11	Absolute Jump	2	2
LJMP	addr16	Long Jump	3	2
SJMP	rel	Short Jump (relative addr)	2	2
JMP	@A+DPTR	Jump indirect relative to the DPTR	1	2
JZ	rel	Jump if Accumulator is Zero	2	2
JNZ	rel	Jump if Accumulator is Not Zero	2	2
JC	rel	Jump if Carry flag is set	2	2
JNC	rel	Jump if No Carry flag	2	2
JB	bit,rel	Jump if direct Bit set	3	2
JNB	bit,rel	Jump if direct Bit Not set	3	2
JBC	bit,rel	Jump if direct Bit is set & Clear bit	3	2
CJNE	A,direct,rel	Compare direct to A & Jump if Not Equal	3	2
CJNE	A,#data,rel	Comp. immed. to A & Jump if Not Equal	3	2
CJNE	Rn,#data,rel	Comp. immed. to reg. & Jump if Not Equal	3	2
CJNE	@Ri,#data,rel	Comp. immed. to ind. & Jump if Not Equal	3	2
DJNZ	Rn,rel	Decrement register & Jump if Not Zero	2	2
DJNZ	direct,rel	Decrement direct & Jump if Not Zero	3	2
NOP		No operation	1	1

Notes on data addressing modes:

Rn	– Working register R0-R7
direct	128 internal RAM locations, any I/O port, control or status register
@Ri	– Indirect internal RAM location addressed by register R0 or R1
#data	– 8-bit constant included in instruction
#data16	– 16-bit constant included as bytes 2 & 3 of instruction
bit	128 software flags, any I/O pin, control or status bit

Notes on program addressing modes:

addr16	– Destination address for LCALL & LJMP may be anywhere within the 64-Kilobyte program memory address space.
addr11	Destination address for ACALL & AJMP will be within the same 2-Kilobyte page of program memory as the first byte of the following instruction.
rel	SJMP and all conditional jumps include an 8-bit offset byte. Range is +127/–128 bytes relative to first byte of the following instruction.

All mnemonics copyrighted © Intel Corporation 1979

Table 2 The complete instruction set of the 8051/8052 series of microcontrollers from Intel.

face (UART) capable of transmitting and receiving data simultaneously. A special data buffer is provided for the asynchronous receiver to speed up communication with serial peripherals.

The serial port can be programmed to operate in 1 of 4 modes, with software-controlled baudrate and data format. All the usual baudrates up to 19,200 can be selected, as well as clock rates up to 1 MHz for use in networks and multiprocessor communication systems. The clock speed selection is effected with the aid of the timer/counters.

Interrupts and the instruction set

The 8051 and 8052 recognize 5 and 6 interrupt sources, respectively: $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$ (programmable for pulse level or pulse edge detection), timer/counters 0 and 1 (and 2 on the 8052), and the serial port. Interrupt programming with 2 priority levels is completely independent of the hardware configuration. Each of the 5 or 6 interrupt sources can be assigned an individual vector (address pointer). Thus, when an interrupt request is received, the processor jumps to the relevant service routine after having saved the contents of the program counter onto the stack. The full instruction set of the controllers in the MCS-51 family is shown in Table 2.

The 8052AH-BASIC

The Type 8052AH-BASIC microcontroller is undoubtedly the most interesting of the MCS-51 family, since it offers an elegant and efficient way of writing control programs for computer-based projects. Intel have loaded the 8 Kbyte ROM in this chip with a powerful BASIC interpreter, while an additional counter/timer, T3, enables split baudrate operation of the serial interface. The BASIC instruction set (version 1.1) is listed in Table 3. On close examination, it is seen that special commands are included for functions otherwise requiring assembly language. After numerous tests and evaluations, it was concluded that the 8052AH-BASIC is eminently suitable for various applications connected with remote data logging, instrumentation and measurement, and industrial process control. The BASIC interpreter is, of course, slow as compared with machine language routines, but has the advantage of being programmable in "normal" language. Also, debugging and editing programs are significantly less difficult, and inexperienced programmers can learn about the processor's capabilities fairly quickly with a minimum of hardware. It is reassuring to know that Intel can supply a 200-page reference manual for 8052AH-BASIC programmers.

Some special features of the 8052AH-BASIC deserve particular attention. The controller can program virtually any type of EPROM if the correct programming voltage is applied to pin $\overline{\text{EA}}$. Both the "old" (50 ms per address) programming standard and several versions of the interactive algorithm are supported—see the last 14 items under **Commands** in Table 3. RAM, ROM and XFER are commands for manipulating and transferring blocks of memory.

The versatily and programming power of the BASIC processor is evident from a number of special **Statements.** BAUD sets the data transfer rate on the previously mentioned additional serial channel. CALL enables calling machine language subroutines from BASIC. CLOCK1 and CLOCK0 control a real-time clock, and CLEARS initializes the data stack, which is primarily used for exchanging machine language parameters, or for storing local variables. Further interesting possibilities are offered by ONTIME, a statement that allows generating an interrupt at a preprogrammed time, ONEX1, for jumping to a subroutine following an $\overline{\text{INT1}}$ interrupt request (interesting because external and timer interrupts can be dealt via BASIC), PH0 and PH1 for printing in hexadecimal format, PUSH and POP for stack manipulation in BASIC, and, finally, PWM for generating a pulse-width modulated signal. The statements also include a number of useful instructions for calling up interpreter routines direct from BASIC: UI1, UI0, UO1 and UO0.

Table 3

COMMANDS	STATEMENTS	OPERATORS
RUN	BAUD	ADD (+)
CONT	CALL	DIVIDE (/)
LIST	CLEAR	EXPONENTIATION (**)
LIST#	CLEAR(S&I)	MULTIPLY (*)
LIST@	CLOCK(1&0)	SUBTRACT (−)
NEW	DATA	LOGICAL AND (.AND.)
NULL	READ	LOGICAL OR (.OR.)
RAM	RESTORE	LOGICAL X-OR (.XOR.)
ROM	DIM	LOGICAL NOT
XFER	DO-WHILE	ABS( )
PROG	DO-UNTIL	INT( )
PROG1	END	SGN( )
PROG2	FOR-TO-STEP	SQR( )
PROG3	NEXT	RND
PROG4	GOSUB	LOG( )
PROG5	RETURN	EXP( )
PROG6	GOTO	SIN( )
FPROG	ON-GOTO	COS( )
FPROG1	ON-GOSUB	TAN( )
FPROG2	IF-THEN-ELSE	ATN( )
FPROG3	INPUT	=, >, >=, <, <=, <>
FPROG4	LET	ASC( )
FPROG5	ONERR	CHR( )
FPROG6	ONEX1	CBY( )
	ONTIME	DBY( )
	PRINT	XBY( )
	PRINT#	GET
	PRINT@	IE
	PH0.	IP
	PH0.#	PORT1
	PH0.@	PCON
	PH1.	RCAP2
	PH1.#	T2CON
	PH1.@	TCON
	PGM	TMOD
	PUSH	TIME
	POP	TIMER0
	PWM	TIMER1
	REM	TIMER2
	RETI	XTAL
	STOP	MTOP
	STRING	LEN
	UI(1&0)	FREE
	U0(1&0)	PI
	LD@	
	ST@	
	IDLE	
	RROM	

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Table 3 The BASIC instruction set of the Type 8052AH-BASIC includes a number of powerful and efficient commands, statements, and operators.

The third column in Table 3, **Operators**, not only lists the well-known arithmetic and logic operations, but also a number of *special function operators*, starting with CBY( ). These operators offer direct control over I/O lines and memory locations. CBY( ) and DBY( ), for instance, give read/write access to the internal program and data memory, respectively. GET allows a character to be read from the serial interface. The remaining special operators, up to and including TIMER2, are intended for reading from and writing to the register indicated by the relevant abbreviation.

Operator XTAL provides the processor with information about the clock frequency used. This is needed to ensure correct operation of the real-time clock.

The status of the memory can be read at all times thanks to operators MTOP, which returns the highest available memory location, LEN, for information on the length of the program, and FREE for the number of available memory locations. Quite remarkably, the 8052AH-BASIC allows BASIC functions to be called up from assembly language. These functions include floating point calculations, complex arithmetic operations, and input-output routines.

The microcontrollers in the MCS-51 series will be at the heart of a number of projects currently under development in the Elektor Electronics design department. Details on availability and programming will be announced in due course.

Th;DM

Source: *Embedded Controller Handbook*. Intel Corporation.

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For distributors in the UK see Infocard 512 in this issue.

TESTING THE INSTRUMENTS OF TOMORROW

by Adrian Morant

The increasing use of digital technology, rather than the previous generation of analogue systems, in both satellite and terrestrial communications, has resulted in a demand for widely differing testing techniques. Even though the integrated services digital network (ISDN) may largely still be in the future, planning for the necessary testing must be carried out in parallel with the planning of the networks themselves.

These needs have been exacerbated by the introduction of fibre optics which allows a single fibre, with its diameter measured in micrometres rather than millimetres, to carry far more traffic than a bunch of coaxial cables, each 10 mm in diameter.

In addition, there have been major technical advances in mobile communications. Here, one of the outcomes is cellular radio, which relies for its operation on sophisticated techniques originally developed for radio equipment for military and defence purposes.

Reliability essential

Whereas previously there were separate networks for voice, telex, data and so on, the trend is towards the one ISDN. The fully digital transmission and switching, plus the integration of a wide range of services on to the one digital network, increase the need for great reliability in the networks.

The requirements become even more stringent since, with the increasing use of computer-to-computer communications, users are demanding a larger degree of network availability.

Nowhere is this more apparent than in the City of London, where the financial community has moved with the deregulation known as the "Big Bang", to electronic trading. With individual deals worth £1 million or more—and the value of an entire day's trading running into thousands of millions—loss of telecommunications is not so much a problem as a disaster.

In these circumstances, testing must be carried out wherever possible, both as a form of preventive maintenance, and in the event of failure. In the latter case, it is frequently cost effective to use what may, at first sight, be excessively sophisticated equipment, because it will provide quicker and better results.

Wide range of users

Marconi Instruments Ltd, one of the traditional names in test equipment, recently announced its data communications analyser model 2871 for detailed error performance testing. It consists of a pattern generator and error detector, plus a powerful processing facility, providing an extensive range of measurement options. The menu driven instrument, which uses a cathode ray tube (CRT) display, provides for both out-of-service and non-intrusive in-service monitoring and testing at up to 150 kbit/s data rates.

It is aimed at three main user groups: digital network support staff involved in maintenance, installation or commissioning activities; telecommunications design and development engineers; and production testing and quality assurance (QA) departments. These users operate in public and private communications carriers, energy utilities, military and government networks. They include also telecommunications equipment suppliers.

Continuous monitoring

Among the special features of the 2871 is the ability to present test results, not only as bit error ratios, but also as detailed information about the type and time of the error occurrence. This is essential when diagnosing fault conditions in telecommunications networks.

In addition, it is designed to carry out 24 hour unattended error performance monitoring. This is of increasing importance for today's users, whose networks operate around the clock but who find difficulty in recruiting the technical staff to maintain them.

Where the distances spanned by telecommunication cables, either going point-to-point or linking switching centres, are more than just a few kilometres, it is necessary to insert electronic equipment to compensate for losses in the cable. With coaxial cables this is typically every five or 10 km. Today's single mode fibre optic cables allow paths of up to 40 km or even more without regenerators, so that when faults in the cable do occur, it is necessary to locate them with some accuracy.

A precise method

The technique used, based on

The Marconi 2871 data communications analyser.

radar, is known as time domain reflectometry (TDR). It relies on the fact that a portion of a signal pulse sent down the cable—electrical in the case of coaxial cables and consisting of light with fibre optics—is reflected back towards the source when it encounters a discontinuity.

This could be an actual cable fault, such as a break in the cable, or a point where there is a slight kink. While it might not be a problem at the time, it could indicate potential trouble for the future.

Knowing the velocity of propagation, that is, the speed of the signal down the cable, the instrument can be calibrated directly in distance of the fault from the sending end where the instrument is sited. The CRT display, together with calibrated digital controls, allows the operator to learn both the location and type of the discontinuity.

Cossor Electronics Ltd had been manufacturing cable TDRs for a number of years before it introduced units for fibre optical applications. In addition to models for the 850 nm wavelength at which the earlier optical systems operated, the company's range now includes the model OTDR 213S, which has been specifically designed to handle single mode fibres at 1300 nm up to distances of 40 km.

Higher frequencies

In addition, the company is launching a new instrument, the OFL 215, designed to operate at the 1550 nm wavelength, which is increasingly being adopted for telecommunications networks because of the lower attenuation window it offers.

The trend in mobile radio systems is to move to ever higher radio frequencies. Farnell Instruments Ltd has produced a communications test set, model CTS520, designed for service and production testing of simplex or duplex radio transceivers, paging equipment and base or relay stations in frequency bands up to 520 MHz.

It provides the measurement capability of nine separate instruments, plus weighting filters and radio frequency (RF) power load, housed in a readily transportable case. They can be used either independently or together to carry out a comprehensive variety of tests.

The instruments include synthesized RF signal generator, RF counter, modulation meter, RF and audio frequency (AF) power meters, AF voltmeter, distortion analyser, signal interference noise and distortion (SINAD) meter, and a selective calling (CTCSS) tone generator.

Many tests

Only four connections are necessary to the device under test, and measurement are displayed on either light emitting diode or analogue meters. An internal loudspeaker is fitted.

With the test set, it is possible to carry out a wide range of tests that normally require a host of separate instruments. Because of the complexity involved, these frequently need to be carried out by more highly skilled technicians.

Farnell also manufactures test gear covering the frequency bands extending to 1 GHz employed by modern cellular radio networks, such as those operating in Britain.

Racal-Dana Instruments Ltd is another important company on the scene. It is part of the Racal Electronics Group, well known throughout the world for tactical radio equipment, some of which employs frequency hopping. Here, the radios change from one channel to another many times a second in a previously agreed pseudorandom sequence to avoid being jammed and, at the same time, to give a degree of communications security.

Quick response

In the same way, when a cellular phone is moved from one cell to an adjoining one, it has to switch on to a channel associated with its new cell. This has to be carried out in a specified and very short period of time. Consequently, test gear used in conjunction with cellular systems must respond quickly enough to meet these requirements.

The Racal-Dana 9087 signal generator, for example, is capable of implementing over 1,000 complete changes of frequency per second in its fast learn mode. It is a complete instrument, offering excellent purity, a wide range of internal and external modulation facilities, and many output amplitudes.

It is an extremely versatile instrument for use in most areas involving frequency agility. Modern advanced instrumentation often involves automatic testing, so the general purpose interface bus (GPIB) compatibility allows the 9087 to be connected into a complete automatic test equipment (ATE) system.

Similarly, the now well established model 1998 frequency counter is a microprocessor based instrument which measures frequency, time intervals and so on over the frequency range to 1.3 GHz and is consequently an ideal instrument for testing modern communications systems, including cellular radio and satellite systems. Again, being GPIB compatible, it is suitable for ATE applications.

EW PRODUCTS • NEW PRODUCTS • NEW

High-stability subminiature crystals

Manufactured by Japanese crystal specialist Citizen Watch Crystal Company using the AT-cut cleavage technique, the operating frequency of Quantelec's new CSA quartz oscillator crystals drift less than ±30 ppm over 70 ° temperature range.

The new crystals, designated the CSA 309 and CSA 310, are available in frequencies from 3.5 to 3.9 MHz and 4 to 20 MHz respectively. All are designed for operation between −10 and +60 °C with negligible frequency drift between +15 and +40 °C.

CSA crystals are housed in a subminiature hermetic package, 9 mm long and 3 mm in diameter, which imparts excellent shock and humidity resistance. They will survive a 75 cm drop on to a hard surface without degrading the electrical performance or affecting the sealing.

Two load capacitances are listed, 16 pF or 30 pF, with a choice of 50 or 500 microwatts optimum drive level. The shunt capacitance is less than 5 pF.

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CHANGE IN TECHNOLOGY FOR THE NAVY

The Royal Navy has introduced the United Kingdom Maritime Coastal Communication System—UKMACCS—into service to satisfy present and future command communication requirements for UK coastal and off-shore sea areas.

The system, which represents an important change in technology and concept for communications, was designed, installed, and commissioned by Marconi Communication Systems. UKMACCS will be controlled from the Primary Coastal System Control—CSC—at Whitehall Naval Communications Centre by remotely controlling transmitters and receivers situated in northern and southern coastal regions. The system provides gapless radio coverage between ships and shore HQ out to a range of 200 nautical miles. There is also a Secondary System Control situated at HMS Forest Moor in Yorkshire. During recent operational trials, UKMACCS proved successful in providing additional centralized radio and telegraphic facilities.

EURO CELLULAR RADIO

Now that France and Federal Germany have agreed to the narrow-band standard for a Pan-European cellular radio system set by the Conference of European Posts and Telecommunications earlier this year, the Department of Trade and Industry has given the go-ahead for a £1 million cellular radio project.

The project, involving British Telecom, Racal, GEC, and Plessey, is expected to produce results by the end of the year.

Two operators, Cellnet and Racal-Vodafone, have been allocated space in the prototype spectrum for testing prototype Pan-European radio equipment and systems.

In the wake of all this activity, Plessey and Racal announced the setting up of Orbitel Mobile Communications, owned equally by them, who will develop infrastructure equipment and mobile radiotelephones for the European system.

The new company, whose workforce is expected to reach 300 by the end of the year, will be headed by Mike Pinches, until his appointment technical director of Racal Telecommunications. (LPS)

Admiral Sir Nicholas Hunt transmitting a message from UKMACCS to the fleet during the UKMACCS opening ceremony at Comcen Whitehall. (Courtesy Marconi Communication Systems)

SATELLITE COMMUNICATIONS FOR THE CONSUMER MOVES CLOSER

The International Maritime Satellite Organization (INMARSAT) has issued final specifications for its Standard-C satellite communications system.

INMARSAT is the 48-country international consortium that operates a system of nine satellites worldwide for the provision of maritime and other mobile communications services.

Main features of the Standard-C system are that it uses very small earth stations weighing only a few kilograms to transmit and receive telex, electronics mail or data to or from practically anywhere in the world, regardless of distance or weather and independent of existing communications facilities. The "C" in Standard-C could stand for consumer because, for the first time, it will give the consumer access to the quality and reliability of satellite communications.

Demonstrations of the Standard-C system would begin during the latter part of this year; sea trials would be held in early 1988, and full service should be available through some coast earth stations during the second half of next year. (LPS)

NEW LIFE-SAVING RESCUEPAGERS FOR RNLI

The Royal National Lifeboat Institution—RNLI—the charity which operates rescue services around the British coastline, is to have a tailor-made communications system that will mean faster call-out for its lifeboats.

The Rescuepage system has been devised by British Telecom Mobile Communications (BTMC) and will replace such traditional call-out devices as explosive flares.

The first batch of 1000—out of a total of 2000—specially adapted Radiopagers is already being delivered to lifeboat stations that at present are hampered by poor communications or cumbersome call-out procedures.

The new procedure will enable an entire crew to be called out through a single telephone call which alerts all their BT Tone Radiopagers. (LPS)

17th MICROWAVE CONFERENCE

The application of microwaves for mobile radio systems, communication satellite systems, radar, radio communications terrestrial systems, and remote sensing will be among the subjects to be covered at the 17th European Microwave Conference in Rome from 7 to 10 September 1987.

Alongside the conference will be an exhibition which will display products from more than 250 manufacturers on its 200 stands.

A workshop on 11 September will explore the subject of present and future terrestrial and satellite microwave communications for mixed and mobile services. (LPS)

Hi-fi VCR from Mitsubishi

Mitsubishi Electric Corporation recently put on the market a new hi-fi VCR whose picture quality almost matches that of one-inch professional equipment. The new unit retails at Y218,000 (about $1,450). The company plans to produce 5,000 units per month.

MAGNETIC REFRIGERATORS FOR SPACE PROGRAMME

Magnetic refrigerators designed to make satellites and other space-based systems more efficient, more reliable and longer-lasting are being developed by the Electro-Optical and Data Systems Group of the Hughes Aircraft Company.

Magnetic refrigerators will cool space-based infra-red sensors and signal processors to lower temperatures than today's gas-cycle coolers can sustain efficiently.

The three-year $4.9 million contract for the design, development and testing of two magnetic refrigerators for the US Strategic Defence Initiative Organization was awarded by the Space Dynamics Laboratory.

Magnetic refrigerators will provide several watts of power at very low temperatures, making new applications possible at temperatures that are currently difficult or costly to obtain. Future extended space missions will require long-wavelength infra-red sensors and other cryogenically-cooled systems to stay chilled for long periods. Similar cooling may be needed for operating high-speed, high-throughput low-power signal processors.

In space, two other possible applications include astronomical observation and power generation. Magnetic refrigerators may also be used for high-speed rail transport and commercial gas-liquefaction.

FIRST COMPUTERIZED BUREAU SYSTEM FOR SATELLITE TRUCK

Texas Television Station WFAA has become the first news station to equip its satellite truck with the Bureau System produced by BASYS International, a subsidiary of Independent Television News—ITN. The installation gives WFAA remote newsroom capabilities directly tied to the news production system by linking the station's DalSat electronic news gathering (ENG) truck to the BASYS system at headquarters.

BASYS systems are already used by over 100 radio and television newsrooms worldwide, including Cable News Network, the National Broadcasting Corporation, the American Broadcasting Company, the British Broadcasting Corporation, and ITN, but WFAA is the first to implement the remote newsroom system. (LPS)

NEWSROOM SYSTEM FOR SWISS RADIO INTERNATIONAL

BASYS International has received an order from Swiss Radio International for the supply of a newsroom computer system capable of dealing with the many languages used by SRI.

The system will allow SRI journalists to view the four different languages in which they take copy, write in all the Roman alphabet languages they use, and also print them.

BASYS has also developed a method by which material generated in the main newsroom can be downloaded to separate personal computers, allowing Arabic journalists and translators a bi-character environment.

This means that virtually all SRI's 24-hour-a-day broadcasts in seven major languages (English, French, German, Italian, Portuguese, Spanish, and Arabic) plus either Romansch or Esperanto, can be computerized.

Similar BASYS systems are already being used by YLE in Finland and by the BBC. (LPS)

TELETEXT SPREADS ITS WINGS FURTHER STILL

Logica has won a further contract from the Swiss Teletext Corporation to extend its Pavane teletext editorial system at Biel. Believed to be already the largest system of its kind in the world, Pavane provides a full teletext and subtitling service in French, German and Italian.

This will be the second Logica teletext system for the Swiss Teletext Corporation. The first accepts data from Telekurs, a financial services information provider.

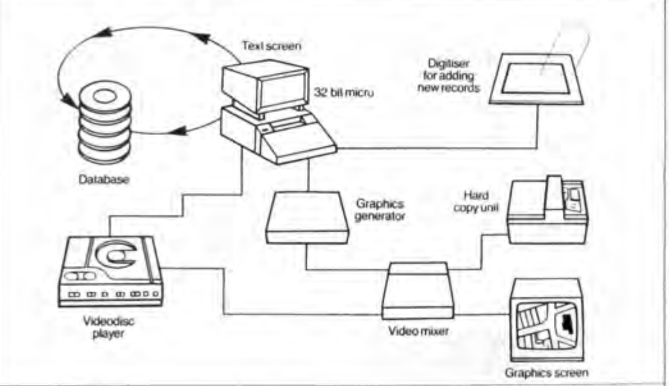
Logica's work on teletext began ten years ago in conjunction with the BBC's CEEFAX service. Since then, Logica has supplied teletext systems to Australia, Austria, Canada, Finland, Germany, Italy, New Zealand, Singapore, Switzerland, and the United States.(LPS)

PUBLIC SECTOR TARGET FOR INFO 88

INFO '88, the eleventh Information Technology and Office Systems Exhibition, will be held next year in the Barbican Exhibition Centre, London, from 7 to 10 June.

During INFO '87, organizer B.E.D. Exhibitions introduced the idea of vertical market days reflecting a developing trend among many business system companies towards specialist selling. INFO '88 will take this marketing approach to a new level for a high technology office systems exhibition.

Aware that the public service sector has special, as well as all-embracing IT needs, B.E.D. is aiming INFO '88 firmly at the largest single group of visitors to attend previous events. (LPS)



Workstation for British Telecom's video map and imaging system — VMIS. This allows ord nance survey maps displayed on a television screen to be overlaid with graphics stored in a microcomputer.

VIDEO MAP AND IMAGING SYSTEM

An advanced interactive videodisc system for displaying maps, plans, or photographs on a TV screen and overlaying extra details by computer was launched recently by British Telecom.

The new product, known as Video Map and Imaging System—VMIS, will offer local authorities, public utilities, emergency services and businesses a powerful and flexible aid to planning and operations.

VMIS is based on British Telecom's M6000 series microcomputer which uses a 32-bit high-speed Motorola MC 68020 microprocessor. The M6000 has been adapted by the company for in-house use on UNIX applications.

To this basic M6000 unit are added a VDU and a keyboard, a graphics generator, a high resolution colour display monitor, digitizer tablet, video mixer subsystem and videodisc unit.

Images are generated and controlled by a Philips VP400 series Laservision videodisc player. Each disc has a capacity of 55,000 photographic images per side. Image retrieval time can be as short as 40 ms.

The operating system is UNIX V.2 and the system software is written in 'C'. UNIX has become the *de facto* operating system for the new generation of super-micro computers.

The main capability of VMIS is its high-speed random selection of an image with the variable data associated with it. The data can take the form of symbols or text, and may be superimposed on the original images.

To simplify this overlay, 64 different levels are available to the user, and these can be recalled in any desired combination.

VMIS can be configured as a stand-alone system or it may networked. The network facility allows a number of workstations to be linked together, as well as giving the product an additional capability of acting as an intelligent terminal.

BRITISH AEROSPACE MESSAGE HANDLING SYSTEM FOR NEW ROYAL FLEET AUXILIARY

British Aerospace Naval and Electronic Systems Division have been awarded a contract by Yarrow Shipbuilders, Glasgow, for the supply of automatic message handling systems for the new Royal Navy Auxiliary Oiler Replenishment (AOR) vessel *RFA Fort Victoria.* The British Aerospace Distributed Message Processing System (DIMPS) uses the latest computer techniques for automating the complete process of message handling on board a modern warship. DIMPS is seen as a critical element in the modernization programme for naval communications and will allow the Royal Navy to capitalize on future increases in radio channel bandwidths and signalling rates, while vastly increasing the accuracy of messages and the efficient distribution of them to all parts of the vessel.

BAe is currently supplying DIMPS for fleetwide use in the Royal Navy's surface vessels and the Submarine Automated Message Handling and Distribution Systems (SAMHADS) for use in the Royal Navy's submarines. The systems for the AOR maintain complete compatibility with other DIMPS fitted vessels providing common logistic support and operational features throughout the Fleet.

CABLE TELEVISION MARKET IN EUROPE

In the face of what Frost & Sullivan's report *Cable Television Market in Europe* (#E904) terms "too many excessively optimistic predictions", it stresses realism. From a 1985 base of 10.05 million European CATV subscribers (5.14 million in the Benelux countries), the report forecasts growth to 12.85 million subscribers in 1987, and 18.4 million subscribers in 1990.

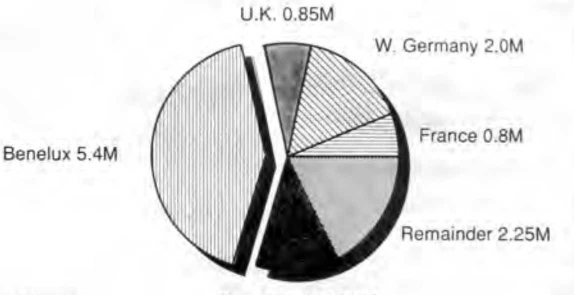
Benelux countries will still lead with 5.7 million, with Federal Germany second with 3.2 million. But the fastest growth rates will be in Scandinavia (from 670,000 in 1985 to 3.1 million in 1990) and France (from 500,000 in 1985 to 2.2 million in 1990).

The report sees overall CATV revenue growing from $680 million (1986 US dollars) in 1985 to $1.3 billion in 1987, and to almost $2.8 billion in 1990. Revenue per subscriber will grow from $85 in 1985 to $100 in 1987, and reaching $150 in 1990.

Since the cost of a full cable TV operation can be as much as $240 per year per home—or as little as $120, depending on the circumstances, the report finds cable operators unlikely to achieve positive cash-flow until year five after start-up, with payback coming around year nine.

The report also looks at the prospects for competing products. For instance, the vast majority of UK households have at least one VCR, so that cable will not quickly gain popularity. In Federal Germany on the other hand, fewer than 50% of households own a VCR, making cable much more popular.

HOMES CONNECTED TO CATV IN EUROPE
1987



SOURCE: Frost & Sullivan, Inc
Report #E904

Life saving communications system

Cut down the time between receiving an alarm call and taking emergency action: that is the requirement of a new alarm centre communication system now under test in Sweden. After only a short period of (test) use, the system has already shown that the time between the alarm call and consequent action can be reduced appreciably.

The system, called Coordcom, integrates and co-ordinates information support and communications handling for alarm centre operators. It has been developed by a subsidiary of Swedish Telecom and will be shown at Telecom '87 in Geneva from 20 to 27 October.

DOUBLE FIRST FOR RACAL AVIONICS

Alaska Airlines of Seatlle is the first US air carrier to purchase the Racal Avionics advanced RNS5000 navigation management system. Racal will provide 19 of the systems for Alaska's Boeing 727 fleet at a cost of £750,000.

The contract is a double first for the British company because, for the first time, the RNS5000 will be used with an inertial reference system (IRS) and a head-up guidance system (HGS).

The secret of the RNS5000's high navigational accuracy lies in its ability to process data simultaneously from a number of different navigation sensors, any of which may be selected to "steer by". More accurate airways by flying on precise go-direct guidance lead to an overall reduction in route mileage with a corresponding saving in operating costs.

ESTEC contract for Signal Processors

The European Satellite Technology Centre—ESTEC—has awarded a contract to Signal Processors of Cambridge for a study on the application of a novel technique invented by SPL to improve sensitivity of ground receivers used to track satellites.

The work will be carried out in collaboration with the SERC's Rutherford Appleton Laboratory which funded the initial work by SPL to validate the new technical approach. Its first application is likely to be in experiments by the European Space Agency with the Olympus satellite, due for launch in 1989, which will operate at much higher frequencies than are employed in current satellite communications.

SPL's approach avoids the use of phase-locked loop signal recovery methods in the receivers. Instead, it exploits digital signal processing by the use of fast Fourier Transform techniques. This is expected to have the additional benefit of lower manufacturing costs.

BOOST FOR CITY TELECOMMUNICATIONS

British Telecom is to spend a further £40 million on optical fibre links for its business customers in the City of London.

In a major step towards completion of the new system, STC Telecommunications, with Plessey as sub-contractor, has been awarded the contract for the second phase of British Telecom's City Fibre Network (CFN), enabling customers to channel all their services through a single "pipeline".

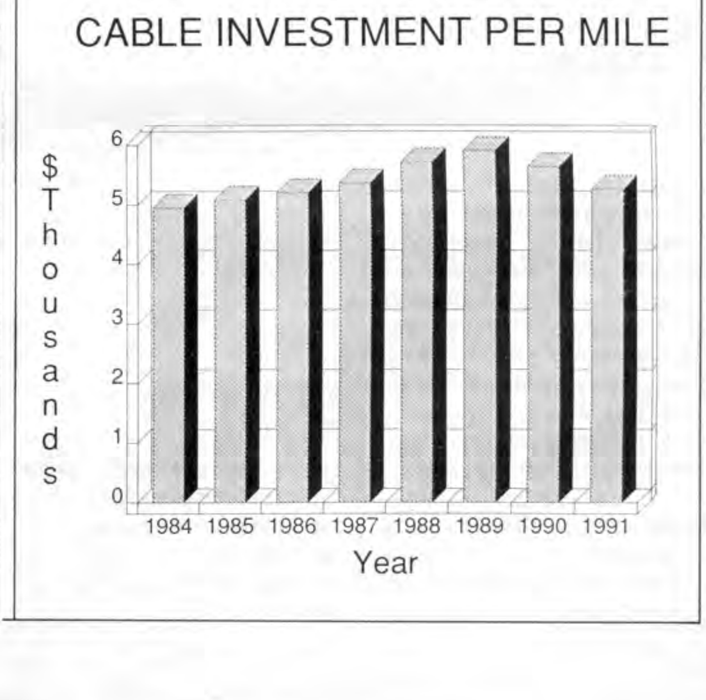
The first phase of the project, announced last December, is nearing completion. Under this £30 million contract, more than 60,000 km of fibre has already been installed, representing the bulk of the CFN cabling.

CABLE TECHNOLOGY FIGHTING BACK

According to *Cable Hardware & Technology Market in the U.S.* (#1653), a study just published completed by Frost & Sullivan, the VCR has been entirely responsible for the drop in cable operator's revenues from pay services. The report notes that the very effective competition of the VCR has forced operators to increase experiments with pay-as-you-view programming, suggesting major growth areas in addressable home converters and in computer systems for billing, tracking, and servicing customers.

Overall, the study says, capital expenditure by the cable operators should grow about 5% a year through 1990, from the $1.5 billion that was spent on equipment in 1986.

About 6,500 cable systems now serve 40 million subscribers; F&S believes the 71,100 miles of plant construction done in 1986 will stand at 74,500 miles in 1990. However, the proportions of new vs replacement plant construction will shift dramatically: new wiring was 55% of the 1986 mileage put in, but will be little more than a tenth of the 1990 figure.



STREAM ENCRYPTION

by B.P. McArdle

One of the evils peculiar to the computerized world is hacking—the unlawful accessing of computers. One way of effectively combatting this nefarious activity is encrypting the data.

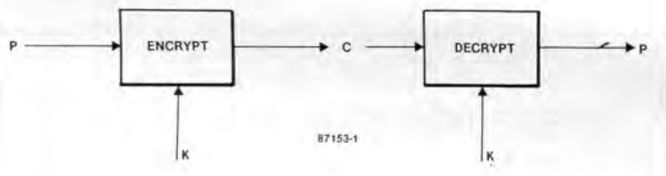
Encryption is the process that turns data into secret form. The original data is known as the plaintext or cleartext and the encrypted data as the ciphertext. If the plaintext is *P* and the ciphertext is *C*, the encryption operation is described by

$$\hat{E}_K\,[P] = C \qquad [1]$$

where *K* is a parameter called the **key** which is used to vary *E*. The effect of a change of key is to generate a different *C* for the same *P*. The user chooses a particular key from a set of possible keys (*K*) and encrypts the plaintext. The ciphertext is stored or transmitted over a channel as illustrated in Fig. 1 to a receiver. The receiving operator must know the particular key in use to enable him to recover the plaintext with the inverse or decryption operation

$$\hat{E}_K^{-1}(C) = \hat{D}_K(C) = P \qquad [2]$$

1



From the point of view of maintaining secrecy, it must be assumed that a cryptanalyst (hacker) would have unlimited ciphertext and would probably know the method of encryption (which means $\hat{E}$), but would not know the particular *K*. To ensure real secrecy, two main tests to assess cryptosystems have evolved over the years:

(a) the set of possible keys must be large enough to make a search with each key in turn impractical. This is called an **Exhaustive Search** and is based on the fact that only the true key will produce meaningful text;

(b) deduction of the true key from known plaintext-ciphertext pairs should be impossible except by an exhaustive search—this is called a **Known Plaintext Analysis**.

Linear functions

A function *f* is said to be linear if it satisfies the following two conditions

(1) $f(x+y) = f(x) + f(y)$

(2) $f(ax) = af(x)$

where *a* is a constant. If these conditions are not met, the function is non-linear. It has been stated that linearity is the friend of the cryptanalyst and the enemy of cryptographers. This statement will become clear later in the article.

Euler's Totient Function

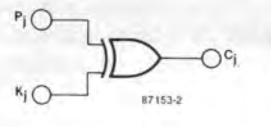
Euler's Totient Function states that $\Phi(n)$ is the number of integers less than *n* that are relatively prime to *n*, that is, have no common factors. For example, $\Phi(31) = 30$.

Stream encryption

In electronic terms, the plaintext is a binary sequence that consists of 1s and 0s. The encryption operation is a **Boolean Exclusive—Or Logic Operation**, illustrated in Fig. 2 where a bit of the plaintext P_j and a key bit K_j are combined in an exclusive-or gate to generate C_j. The operation is described mathematically by

$$C_j = (P_j + K_j) \bmod 2 \qquad [3]$$

2



The reasons for using this operation as opposed to OR or AND are that *C* is 0 or 1 with equal frequency and that the decryption operation only requires the same operation:

$$P_j = (C_j + K_j) \bmod 2 \qquad [4]$$

The following example for encrypting/decrypting five bits explains the overall procedure

Encryption operation

P_j : 1 0 1 0 1

K_j : 0 1 1 0 0

$P_j + K_j$: 1 1 2 0 1

$(P_j + K_j) \bmod 2$: 1 1 0 0 1

Decryption operation

C_j : 1 1 0 0 1

K_j : 0 1 1 0 0

$C_j + K_j$: 1 2 1 0 1

$(C_j + K_j) \bmod 2$: 1 0 1 0 1

To summarize, a stream cryptosystem is essentially a deterministic process for generating a key sequence (K_j) which should have approximately equal numbers of 1s and 0s, and have a very long period so as to appear random to an observer.

Linear-feedback shift registers

A linear-feedback shift register is illustrated in Fig. 3. Each stage is a JK bistable (flip-flop). The output is taken from the last stage. The feedback function generates successive states from an initial state or **seed** as follows:

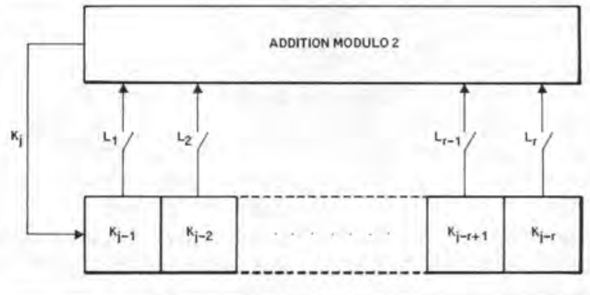
$$K_j = f(K_{j-1}, K_{j-2}, \ldots, K_{j-r}) \quad \text{for } j > r \qquad [5]$$

which for a linear-feedback arrangement may be rewritten as

$$K_j = \sum_{i=1}^{r} (L_i K_{j-1}) \bmod 2 \text{ for } j > r \qquad [6]$$

$$L_i = 1 \text{ for latch i closed} \qquad [7]$$

3



$L_i=0$ for latch i open [8]

To ensure that (K_j) has an approximately equal number of 1s and 0s, latch r is usually left closed. If, for example, $r=5$ with L_3 open and the other latches closed, the linearity of f can be shown by the following results:

$f(1,0,1,0,1)=0$ [9]

$f(1,1,1,1,0)=1$ [10]

$f(0,1,0,1,1)=1$ [11]

The 3rd state on the left can be generated from a modulo 2 addition or an exclusive-OR between the other 2 states. The same result can be obtained on the right-hand side. Thus, the arrangement satisfies the first condition for a linear function. There is no need to consider the second condition, since a is 0 or 1 in modulo 2 arithmetic. Note, however, that the state "all 0s" always generates itself.
In the operation of the shift register, each state has a unique predecessor and successor. The total number of possible states for r stages is 2^r, but the state "all 0s" is never used, which means that the maximum possible period is 2^r-1. In the previous example, the key sequence from a seed (1,0,1,0,1) is (1,0,1,0,1,0,0,1,0,0,0,1,0,1,1,1,1,1,0,1, 1,0,0,1,1,1,0,0,0,0,1) and has a period 31, which means that the choice of latches results in maximum period. Obviously, not every arrangement of the latches produces maximum period. There are $\Phi(2^r-1)/r$ different arrangements, where Φ is Euler's Totient Function. For $r=5$, this gives $\Phi(2^5-1)/5=6$.
In encryption applications, the question of secrecy must be examined. If a cryptanalyst knows the value of r and the last 10 bits of the key, he can construct the following sequence of states:

0 — (1,1,1,0,0)

0 — (0,1,1,1,0)

0 — (0,0,1,1,1)

0 — (0,0,0,1,1)

1 — (0,0,0,0,1)

and these 5 equations:

$0=(L_1+L_2+L_3) \bmod 2$ [12]

$0=(L_2+L_3+L_4) \bmod 2$ [13]

$0=(L_3+L_4+L_5) \bmod 2$ [14]

$0=(L_4+L_5) \bmod 2$ [15]

$1=L_5 \bmod 2$ [16]

From Eq. [16], $L_5=1$. Therefore, Eq. [15] can be rewritten as

$0=(L_4+1) \bmod 2$ [17]

which gives $L_4=1$. Continuing in this manner gives $L_3=0$ and $L_1=L_2=1$.
The mathematical problem can also be formulated in matrix form such that the solution requires the calculation of the inverse matrix. This method is more suitable for large values of r, because a cryptanalyst could make use of computer packages. But once the latch arrangement and a state for the shift register are known, the full sequence can be generated. Consequently, the linear function, irrespective of the value of r, is too predictable for secrecy and does not satisfy test 2.

Shift register with non-linear logic

In the shift register with non-linear feedback logic—see Fig. 4—the incoming bit is generated according to

$K_j=f(K_{j-1},K_{j-2},\ldots,K_{j-r}) \bmod 2$ [18]

where f is a non-linear function. Normally, f is chosen such that

$K_j=[f'(K_{j-1},K_{j-2},\ldots,K_{j-r+1})+K_{j-r}] \bmod 2$ [19]

which ensures that (K_j) has approximately equal numbers of 1s and 0s.
The new function, f' is also non-linear, which is made clear by the following example. If,

$K_j=(K_{j-1}K_{j-4}+\overline{K}_{j-2}\overline{K}_{j-3}+K_{j-5}) \bmod 2$ [20]

then,

$f'(1,0,1,0,1)=1$ [21]

$f'(0,1,0,1,0)=0$ [22]

$f'(1,1,1,1,1)=0$ [23]

An exclusive-OR between the 1st and 2nd states on the left gives the 3rd, but the same operation on the right gives 1 instead of 0, which shows that the feedback function is non-linear. It appears to be more complex than the linear arrangement and the reader would be justified in assuming at first glance that it is also more secure. For a seed (1,0,1,0,1), the key sequence for the first 31 terms is (1,0,1,0,1,1,1,1, 1,0,1,0,1,1,1,1,1,0,1,0,1,1,1,1,1,0,1,0,1, 1,1). However, the period is short and the sequence repeats more than once. A more detailed examination shows that the **sequence of states** has 6 cycles:

00000-10000-11000-01100-00110-00011-00001

00010-10001-01000-00100

10101-11010-11101-11110-11111-01111-10111-01011

01101-10110-11011

00101-10010-01001-10100-01010

11100-01110-00111-10011-11001

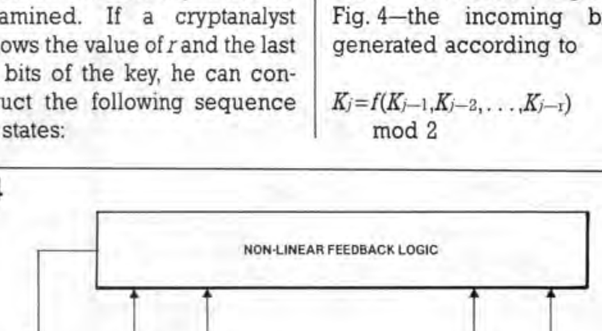
An interesting point is that the state (0,0,0,0,0) does not generate itself. From the point of secrecy, the key sequence actually has period 8 and repeats 3 times within the 31 terms. Thus, non-linear functions are **not necessarily** more secure than the linear variety. But no such cryptosystem, irrespective of the period, offers any real secrecy. If a cryptanalyst knows the feedback function, he can generate the balance of the sequence following r known bits. Consequently, this arrangement also fails test 2.
The arrangement of Fig. 5 attempts to eliminate the two main weaknesses. The linear feedback function generates the incoming bits to the shift register and consequently determines the period of the entire system. The non-linear feed-forward function generates the key bits and protects the shift register from an analysis with known key bits. The two previous examples combined result in

$K_j=(K_{j+4}K_{j+1}+\overline{K}_{j+3}\overline{K}_{j+2}+K_j) \bmod 2$ [24]

$K_{j+5}=(K_{j+4}+K_{j+3}+K_{j+1}+K_j) \bmod 2$ [25]

For the seed (1,0,1,0,1), the key sequence is (1,0,1,0,1,0,1,0,0,0,1,1, 1,0,1,0,0,1,0,1,1,0,0,1,0,0,1,0,0,1,1) and has period 31. The secrecy depends on the cryptanalyst not being able to deduce K_j to

4



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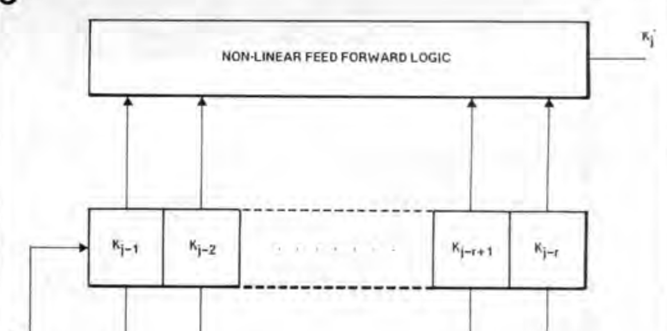


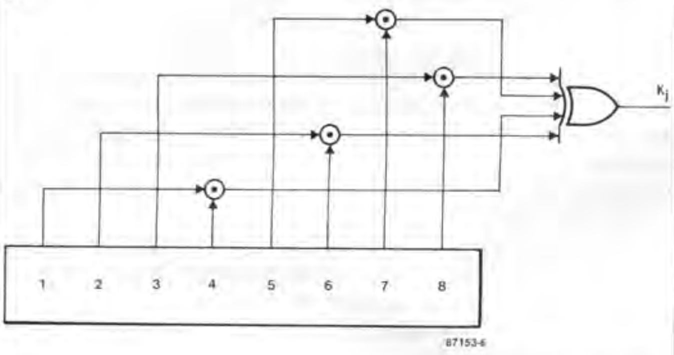
K_{j+4} from K'_j to K'_{j+4} (assuming a worst case analysis where both functions are known). In this simple example, such a deduction is turgid rather than impossible. But an actual commercial system would have $r=128$ or $r=256$. In designing such a system, the feedback logic would be one of $\Phi(2^r-1)/r$ latch arrangements that produce a maximum period of 2^r-1.

The non-linear logic could be chosen with a variety of methods, but the following is simple and straightforward. In Fig. 6, the output or inverted output of each stage (bistable) is connected to an AND gate with the constraints:

(a) each gate has only 2 inputs;

(b) the span of the inputs does not exceed the number of stages.

6



For example, the pairs 1-4, 2-6, 3-8, and 5-7 satisfy these conditions. The resulting function is not necessarily non-linear in the strict mathematical sense, but for a large value of r, it would be quite complex. A cryptanalyst would have to discover a method of solving equations which have non-linear operations or use an exhaustive search. For $r=256$, this would be impractical. Therefore, this arrangement is reasonably secure. A useful hint for designers is to include a facility to vary the logic arrangements such that the same functions are not used too often.

Congruence generators

The congruence generator method is essentially a computer algorithm for generating a sequence of numbers from a seed X_0 as follows:

number sequence

$$X_j=(AX+B) \bmod M \qquad [26]$$

binary sequence

$$K_j=X_j \bmod M \qquad [27]$$

Thus, K is 0 or 1, depending on whether X is even or odd. The modulus, M, is the largest prime that can be fitted to the processor's word size, while A and B are integral powers of some prime factor. The generated sequences are periodic, because once the seed is reproduced, the complete succession of results after the seed also repeats. For example, $X_0=8191$ $A=13{,}077$; $B=-6925$; $M=32{,}767$ has period 1050. But the simplicity of the operation is also its weakness. Generally, A, B, and M are machine constraints, which means that X_0 is the only parameter that is varied. In addition, some seeds have short periods which in turn limits the choice of seed. In applying test 2, it must be assumed that a cryptanalyst would have all the details except the seed. Thus, the secrecy depends on the difficulty of deducing X_j from K_j. For instance, if $K_j=1$, for a 16-bit word, X_j is an uneven number between 1 and $2^{16}-1$. An examination which would try each possible number in turn in Eq. [26] would **not** be impractical. Consequently, this system implemented on the standard desk-top would not satisfy test 2.

X^2 mod PQ generator

In this method, a sequence of numbers (X_j) is generated from a seed X_0 as follows:

number sequence

$$X_j=X_{j-1} \bmod N$$

binary sequence

$$K_j=K_{j-1} \bmod 2$$

The modulus, N, is the product of two large primes P and Q that are congruent to 3 mod 4 and $gcd(X_0,N)=1$. Therefore, K_j is 0 or 1 depending on whether X_j is even or odd. The set of possible seeds has $\Phi(N)=(P-1)(Q-1)$ elements, where Φ is Euler's Totient Function. The main difficulty here is implementation on desk-top microcomputers which normally handle 12-digit numbers. For secrecy, P and Q must be very large primes in the order of 100 digits. Consequently, the method is considered to be suitable only for Public Key Encryption, which is **not** covered in this article.

Measurements of ventricular distances by using ultrasonic techniques

by Baki Koyuncu (Physics Department, Kuwait University, Kuwait)

A well known technique was used to determine the external dimensions of the heart on any one of its cross-sectional planes under clinical conditions. The circuit described here used sound radiation in liquid and biological media. Sound was transmitted and received by two PZT-4 transducers placed on opposite sides of the sample heart. The time taken by sound to travel through the medium at a known speed V, was measured electronically. The distance between two transducers was calculated from d = Vxt.

Under clinical conditions, measurements of distances between surface points of a heart are required. This information is coupled with pressure, blood flow, muscle contraction, etc and contributes towards the diagnostic picture of the heart.

Numerous techniques (1,3) with implanted radio-opaque markers have been used to assess global cardiac function both before and after operative procedures. Moreover, attempts have also been made to quantify the dimension changes by means of indirect methods derived from ventricular pressure contours (5-7). The system developed here employs small oscillating piezoelectric crystals which may be implanted or sutured epicardially. Thus stable, independent alignment of transducers becomes possible and allows precise acquisition of dynamic dimension variations. PZT-4 transducers were placed successfully around the heart to evaluate the ventricular regional function in patients during the experiments.

In this study detailed dimensional changes were quantified. It was confirmed that the system responded predictably to external stimulation as well as alterations in ventricular preload and afterload. Electronic design procedures are presented here together with details of transducer construction. Experiments were carried out on animal hearts for a variety of clinical situations.

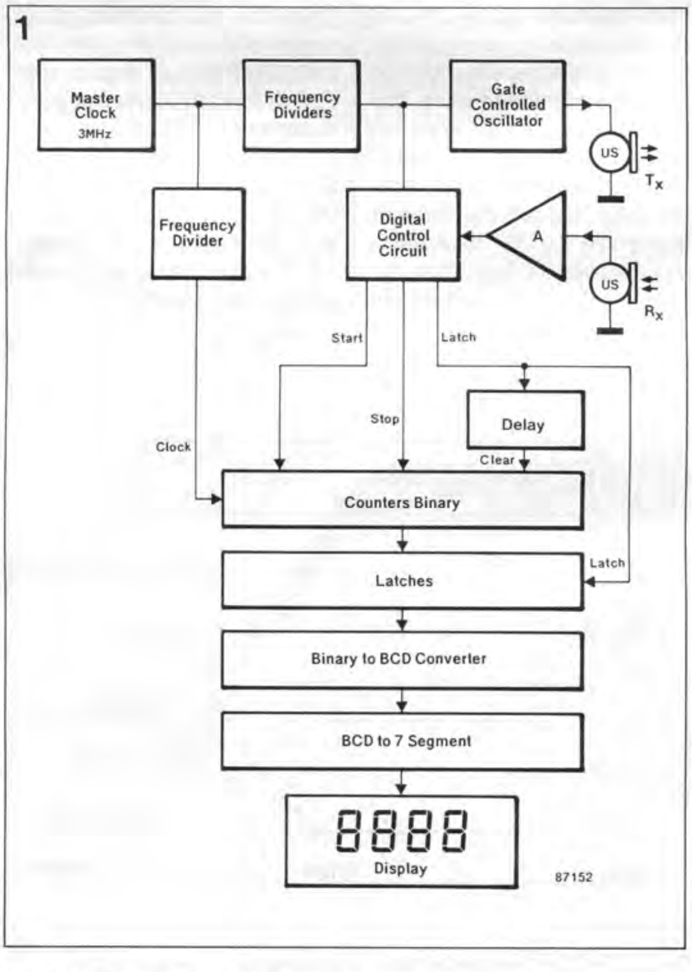


Fig. 1. Block diagram of the complete system.

Method

The PZT-4 transducers employed during this study were made of barium titanite (Ba Ti O3). They were in rectangular shape with radiating surface dimensions of 10 mm by 10 mm. Two identical transducers were used. One was for transmission (Tx) and the other for reception (Rx) of sound waves. Each was placed in a plastic casing in such a way that half of its height was outside the case. An air cavity was produced between the casing and the transducer by sealing all the edges of the transducer with a silicon based epoxy glue. The whole unit simulated an air backed transducer. Sound radiated from the back radiating surface was reflected back from the air-transducer interface and transmitted from the front radiating surface hence doubling the transmission energy. Copper wire electrodes were attached on both surfaces and transmission voltages were applied across them. A fundamental resonant frequency of 300 kHz was chosen for these transducers. The transducers were implanted externally on opposite sides of the heart. Their weights were small enough to justify assuming that they did not damp the motion of the heart.

A glass tank with dimensions of 1 m × 0.5 m was used for the experiments. The sample was suspended by mechanical clamps in mid air and submerged into the tank. The tank was filled with air and it provided a stable environment free of temperature, air, etc. fluctuations.

A train of pulse bursts was generated from a gate controlled oscillator. Peak voltages corresponding to these pulses were applied across the Tx transducer at its resonant frequency. The tranducer impedance across its terminals was measured at resonance as 30 Ω in air. The transmitted pulses had a duration of 5 μs and a repetition frequency of 1.5 Hz. The amplitude of the applied voltage was 9 V; hence the transmitted signal power level was $(9/\sqrt{2})^2/30 = 0.7$ W. Detection of the transmitted sound radiation was carried out by an identical transducer (Rx). The received pulses were amplified and used to generate START, STOP and LATCH control pulses.

The block diagram of the complete system is presented in Fig. 1. Start pulses indicated the start of the transmission and activated the counters to count the clock pulses corresponding to the unknown distance. Stop pulses were generated when the transmission was received by Rx. They deactivated the above counters counting the clock pulses. Hence the counters contained a particular number of counts representing the distance between Tx and Rx.

A 5 μs duration pulse was produced at every half cycle of 1.5 Hz. These pulses were termed 'latch pulses' and used to reset the counters for the next count sequence. The final count at the counter outputs were also transferred to the latch and display sections of the was also transferred to the latch and display sections of the circuit by means of latch pulses. Timing diagrams of the different pulses are illustrated in Fig. 2.

Circuit description:

Complete circuitry of the system is shown in Fig. 3. A FET collector feedback oscillator with its amplifier was used as master clock. A 3 MHz crystal was used along its feedback path to generate 3 MHz sinewave oscillations. The output was EX-OR gated to convert the oscillations into digital form. These pulses provided the synchronization throughout the system and the control pulses were derived from them. The oscillator frequency was divided by 2×10^6 by decade counters and a JK flip-flop. The frequency divider chain provided a square wave train output with a frequency of 1.5 Hz (corresponding to a period of T=666 μs). An RC combination with a 1.5 V dc offset differentiated the square wave and shifted the resultant above zero volt. A Schmidt trigger gate, N1, produced the latch pulse with 5 μs duration at every half cycle of 1.5 Hz.

The 1.5 Hz square wave was inverted by N2. A Schmidt trigger gate, N3, gave an output pulse with 5 μs duration at the beginning of every 1.5 Hz cycle. Its input was the RC differentiated N2 output. These pulses, termed 'start pulses', were applied to the gate terminal of the Tx oscillator (N4 gate) as trigger pulses. The frequency of the Tx oscillator was set to the resonant frequency of the transducer. The transducer was activated for duration of the start pulse. Hence, a pulse burst of 1.5 cycles at 300 kHz was transmitted with the application of the start pulse. The received pulses at the receiver were time delayed due to the finite distance travelled by the sound. The transmitted pulses also appeared at the receiver due to the electronic interference. The inverted start pulses were applied to multivibrators 1 and 2. The first multivibrator's negative edge trigged the inverted start pulse. Its RC time delay was adjusted to 7 μs. Then the output pulse was used to envelope the unwanted transmitted pulse section of the received pulse train. A 7 μs pulse width set up the limit for minimum distance measurement. It corresponded to approximately $7\times10^{-6}\times1500=10.5$ mm distance.

The negative edge of multivibrator 2 triggered the output of multivibrator 1 and produced a digital high. Later, the output was AND-gated by N6 and N7 with the received pulse train. Consequently, the output of N7 contained only the received pulses corresponding to the distance travelled without any interference present. The output of N7 was positive edge triggered by multivibrator 3 and 4 to produce a stop pulse of 5 μs duration. Start, stop and latch pulses were used to control the counters. Initially, a 1.5 MHz signal was applied as the clock signal to the counters. This was derived by dividing the 3 MHz master clock signal by 2. The velocity of sound in the medium was taken as 1500 m/s from the literature. Thus, a conversion factor $\alpha=1$ mm/cycle was introduced for the counters. This meant that 1 mm distance corresponded to 1 count cycle of the counters. Therefore, the counters would count whole cycles and the numerical display would give straightforward distance measurements in millimeters.

The start pulse was applied to D flip flop (1) as a clock. When D=1, the Q output was set HIGH and the output of N8 copied 1.5 MHz from its input. The output of D flip flop (2) was also set HIGH when a stop pulse was applied as a clock. Therefore, N8 output was transferred to N9 output and applied to counters as clock signal. D flip flops had the inverted latch pulses as their CLR (clear) and PS (preset) inputs. These inputs normally stayed HIGH to let the 1.5 MHz counter clock pulses go through the D flip flops.

When the latch pulses arrived, D flip flop (1) output was reset to LOW. D flip-flop (2) output was preset to receive the next count sequence. The clock pulse train between the start and stop pulses corresponding to a particular distance count were applied to the counter stage. Counters were 4-bit binary counters connected in series to give a maximum count of 2^{11} at its 12 outputs. Delayed latch pulses were applied to the CLR inputs of the counters. A delay of approximately 60 ns was introduced to avoid the counters being cleared at the same instant as the D flip-flops. Otherwise, the count would be lost before it was latched by the latch circuits.

Transparent latches were enabled by the latch pulses. Twelve-bit latch outputs in binary form represented the final number of counts corresponding to the millimetre distance between two transducers. These 12-bit binary numbers were converted to BCD numbers by binary-to-BCD converters and later displayed by 7-segment display units. A variable capacitor C was introduced in series with the master oscillator crystal. It was used to compensate for the frequency changes due to sound velocity irregularities in the medium.

Exact velocity of sound was calculated as 1550 m/s in the experiments. Hence the master clock frequency was adjusted to 3.1 MHz by changing the C value. The new clock frequency for the counters was thus 3.1 MHz÷2 = 1.55 MHz. As a result, the counter conversion factor (α) remained 1550 m/s÷1.55 M cycle/sec = 1 mm/cycle and 1 mm distance would again correspond to 1 count cycle of the counter.

Calibration of the whole system was carried out along the same lines. In the test medium, a precise distance between the Tx and Rx was set by mechanical means. The test medium was

2

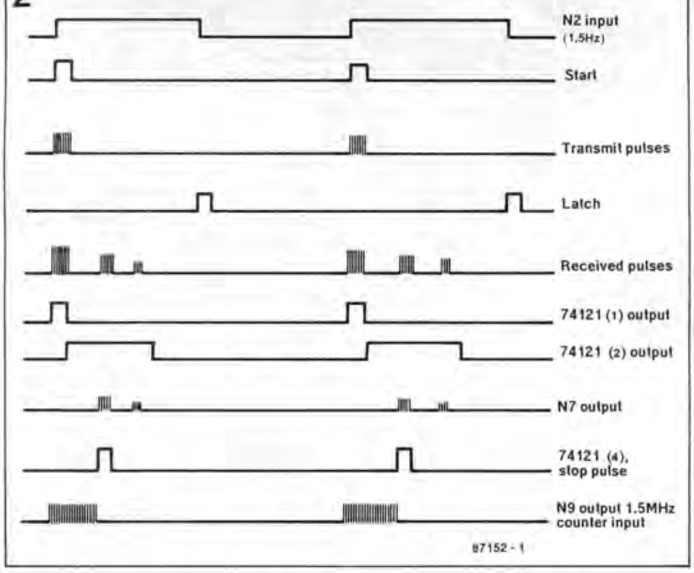


Fig. 2. Timing diagram of different pulses and frequencies present at various points in the circuit.

blood and the distance was set to 30 mm. The display unit readout was adjusted by changing the value of the capacitor in the master oscillator until the display read 30. Similar calibration measurements were made with the stationary heart filled with blood. It was found that the displayed numerical values were consistently the same as the mechanical measurements. Hence, the whole system was ready to measure the dynamic distances in the experiments.

Experimental Considerations

Motion of the heart is a three-dimensional complex motion. The circuit described here would only give the shortest distance along a particular direction between the transducers. The Rx transducer always detected the maximum radiated sound intensity along this direction.

The minimum distance measured was governed by the outputs of multivibrators 1 and 2 and was set to 10.9 mm. Counting was incremented in steps of 1 and the distance was incremented in steps of 1 mm. If the count was more than 0.5 but less than 1, it was approximated to 1 count. If it was less than or equal to 0.5, it was disregarded. Consequently, the maximum uncertainty introduced was 0.5 count corresponding to 500 μm. This error could be reduced by counting more cycles for 1 mm distance. For example, if the 3 MHz master clock frequency was counted, the conversion factor would be 0.5 mm/cycle (2 count cycles per mm) and the above error would be 250 μm. Further increases in frequency would improve the accuracy of the measurement, i.e. 6 MHz would allow a distance step size of 0.125 mm to be measured. This would give an uncertainty of 0.06 mm (if one could position the transducer this accurately!). For clinical purposes distance measurements with ±500 μm uncertainty were sufficient. Hence, no improvement in accuracy was attempted.

The maximum measurable distance corresponded to the time interval between start and latch pulses; and it was equal to ½ × 1/1.5 = 0.333 second. If each count represented the time increment tc = 1/1.5 MHz = 0.66 μs, the maximum number of counts between these pulses would be 0.333 sec/0.66 μs = 5.05 × 10^5. Hence, a theoretical distance of 505 m

3

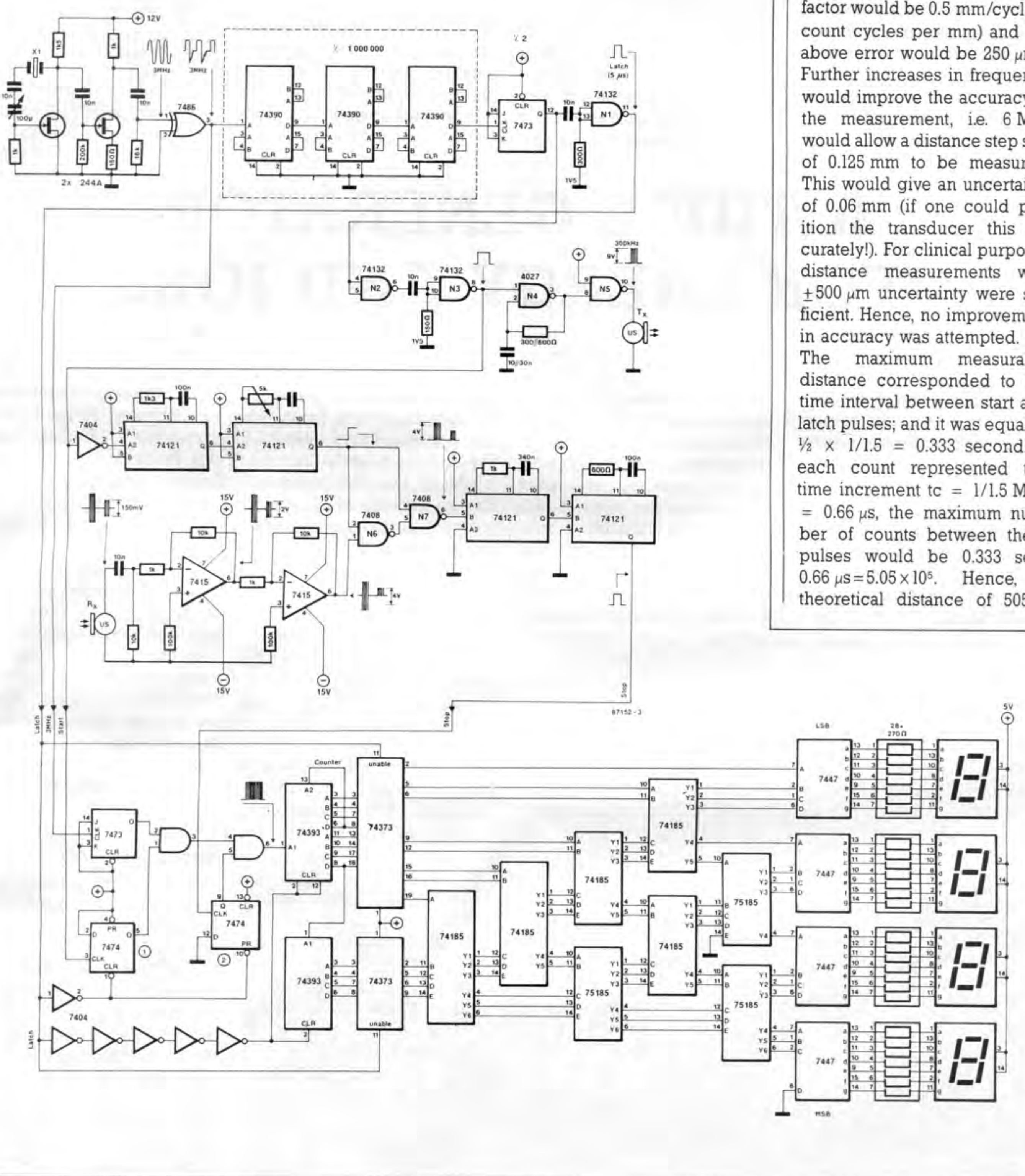


Fig. 3. Circuit diagram of the complete system.

would be displayed by the display units.

The transmitted power levels would set a more stringent limit on large distance measurements. The power received by Rx would decrease rapidly with the increasing distance. Since heart dimensions of 50-150 mm were measured, power considerations were not a limitation on the experiments. The system was in no way comparable to X-Ray tomography, emission tomography or some other advanced ultrasonic devices. These are used for non-invasive clinical applications to man and they are far superior in distance measurements to the system here. The system constructed was solely used in the laboratory to give some notional data of the heart simply and efficiently. It could quite easily be used for any biological sample, once the sound velocity in it was known.

A large signal amplitude was always present at the receiver terminals corresponding to the minimum path through the heart. Other reflections from the side walls were small compared to the main received signal. The circuit did not include automatic gain control in the receiver stage or automatic error compensation (comparing a number of consecutive readings for the same distance) to keep it as simple as possible. Counters were reset by the positive going edge of the delayed latch pulses allowing a new measurement to be taken at every 0.66 seconds.

The previous read-out remained on the display until the information from a new distance measurement arrived. Finally, the accuracy of the measurements was dependent on the factors which influence the speed of sound. The range of the instrument could be extended by increasing the gain of the receiver and the transmitter voltage. This was unnecessary for the measurements described here.

Acknowledgement

The author appreciates the help received from the Physics Department of Kuwait University. The work was carried out under a SDP 111 grant.

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A TIDAL GENERATOR FOR ENERGY AND JOBS

by Vic French

An ambitious plan to produce electricity from a tidal barrage acros the River Severn estuary has been investigated by a special body reporting to the Secretary of State for Energy. The barrage might run from the holiday resort of Weston-super-Mare to Cardiff, though the study also considers an alternative location.

Coincidental with the report—submitted by the Severn Tidal Power Group (STPG)—was a government pledge backing further studies in tidal resources to the value of £5.5 million. This includes a contribution towards research into a River Mersey barrage with generic studies to take in construction techniques and an investigation into the potential of smaller sites around Britain.

The Severn scheme investigation and report were financed jointly by the Department of Energy with the STPG, and a group of companies comprising Sir Robert McAlpine and Sons, Balfour Beatty, GEC Energy Systems, Northern Engineering Industries (NEI), Taylor Woodrow Construction and Wimpey Major Projects (representing Wimpey Atkins Joint Venture).

Among attractions of the scheme are the facts that it would contribute up to 6% of the demand for electricity in England and Wales, would have a life of at least 100 years, and could provide a trunk road across the Severn estuary to link the present and proposed major road networks in south-west England and south Wales, relieving the Severn Bridge.

Its generation costs would be comparable to those of the Sizewell B nuclear power station.

An artist's impression of the Cardiff-Weston barrage looking upriver.

Second option

The study has considered a second option for a barrage adjacent to English Stones, a site some eight kilometres from the Severn Bridge and 36 km upriver from the Weston-Cardiff site. A potential problem there is that fine sediments might affect the barrage, and a major investigative study would be required.

The capital cost of the Cardiff-Weston scheme is estimated at £5,543 million (January 1984 prices). It could provide 45,000 jobs during the construction

PRINCIPAL DETAILS OF THE SCHEMES

	Cardiff-Weston	**English Stones**
Total length of barrage	16.3 km	7.1 km
Installed capacity	7,200 MW	972 MW
Type of turbine generator	Bulb	Bulb
Number of turbine generators	192	36
Runner diameter	8.2 m	7.5 m
Effective sluice area	21,600 m²	5,976 m²
Number of turbine generator caissons	48	12
Turbine generators per caisson	4	3
Plain caissons in lieu of embankment	50	2
Annual energy sent out (average year)	14.4 TWh	2.8 TWh
Capital cost (January 1984)	£5,543 million	£1,150 million

period of seven years, with at least another 22,000 jobs outside the energy sector. About 1,700 people would be directly employed to operate the scheme, and there would be considerable benefits in the form of industry, housing and tourism.

The proposed Cardiff-Weston barrage would have a length of 16.3 km, with an installed capacity of 7200 MW from 192 bulb turbine generators in runners of 8.2 m diameter. There would be 48 turbine generator caissons, each 65 m by 72 m in plan, with four turbine generators per caisson and an effective sluice area of 21,600 m². The annual energy output would total 14,4 terawatt hours (TWh), one terawatt hour being a million million kilowatt hours.

Siltation studies by STPG have shown that it will be necessary to use empty caissons to close the barrage on either side of the turbine caissons instead of the more normal embankments. They would be watertight structures open at the bottom and containing air under pressure. There would also be 62 sluice caissons and 50 plain caissons.

The advantages

A total volume of structural concrete of 3.1 million m³ would be required. Steel structures have been considered but do not show any cost benefit over concrete. An internal structure of steel might be an advantage but this would need investigation.

Plain caissons used instead of embankments are recommended where the seabed level is even lower than 15 metres below the Ordnance Datum level, as this reduces the total volume of materials required for construction, speeds up the time taken for the work, and improves the closure sequence.

The type of turbine generator has been chosen in view of the long operational experience with this particular design. It could be manufactured with the certain knowledge of its performance and installed as a complete package. The 1600 tonne package would be constructed as a single unit, floated to site on a sea-going barge, and installed in the caisson which could already be in position in the estuary. This would be a considerable advantage, as the plant would be factory tested and partially commissioned, reducing the time and manhours required for installation in the barrage.

The number of turbine generators used in the barrage, of course, controls the "energy capture" of the scheme, but would be restricted by the available depth of channel in which they could be located without the need for expensive dredging.

Variable speed DC generation has been considered in the quest for an improvement in economy, but the gain in energy produced was smaller than expected, and the cost of a high voltage DC system would not be recovered by increased revenue or significant operational benefits. Fixed speed generation and AC transmission have therefore been chosen.

Not a problem

Re-inforcement of the Central Electricity Generating Board (CEGB) transmission system would be required to accommodate the output from the barrage. This would be undertaken by the CEGB and financed from barrage revenue. Intermittent output from the barrage would not pose a major problem as power stations have to contend with much larger power variations in consumer demand.

In order to increase the net value of annual energy put out by an ebb generation barrage, the STPG considers that there would be a net benefit in pumping into the basin at neap and mean tides.

There is a proposal for a smaller schema with a barrage to be built some eight kilometres downstream of the Severn Bridge. This too could carry a trunk road across the Severn estuary to link Wales with southwest England. The cost of this English Stones scheme would be £1,150 million (January 1984 prices).

Bulb turbine generators would also be used for this scheme, with 36 installed in 12 caissons, each 63 m by 50 m in plan. The diameter of the turbines would be 7.5 m each with a rating of 27 MW and a total installed capacity of 972 MW. There would be 42 sluices in all, of which 30 would be 12 m × 11 m and 12 would be 12 m × 14 m. Ebb generation with flood pumping would be used again here, giving a firm power contribution of 250 MW and an average annual energy output of 2.8 TWh.

Needs of shipping

Barrage construction would be very similar to that at Cardiff-Weston although embankments would complete the barrage on each side of the turbines and sluices.

In both cases consideration would have to be given to the requirements of shipping. It is suggested that two alternative lock sizes should be constructed, one for vessels up to 6,000 dead-weight tonnes and one for larger ones of up to 25,000 dwt. The locks would be situated between sluice caissons on the Welsh side. This takes into consideration the prevailing wind and current conditions expected when the scheme is complete.

The STPG considers that the larger scheme between Weston and Cardiff would be a great asset to the United Kingdom, with its potential for creating employment and the fact that it would produce virtually free energy as an insurance against unpredictable increases in primary energy costs. Tidal power is also non-polluting to the environment.

68000 microprocessor trainer links to BBC Micro

The Flight Electronics 68000 microprocessor trainer (FLT-68k) can now be linked to a BBC microcomputer, so that users can learn 68000 programming and develop 68000 applications in the familiar BBC environment.

The FLT-68k's high-speed in-line assembler and efficient debugging facilities are easily accessed from the BBC micro. The computer and monitor act as a terminal and control console, connected via the serial port. A printer can also be attached, for hard-copy output.

A powerful cross-assembler package is available, enabling 68000 object code to be generated on the BBC micro and downloaded to the FLT-68k trainer. The package allows high-speed assembly, using standard Motorola mnemonics throughout. The object code files may be formatted in absolute binary, or Motorola 'S' format.

Files can be sent to disk or to the FLT-68k. Source code modules can be stored on disk for assembler recall, and can be included in other source code modules.

By defining labels, symbols, and variables as local to a source code module, up to 4 Mbytes of source code can be assembled. Other features include user defined listing format, full range of pseudo ops, and a help facility which displays the entire 68000 instruction set.

The cross-assembler package includes a 16 Kbyte EPROM, two utilities diskettes, and a comprehensive instruction manual. The EPROM is compatible with BBC B, and Master series machines. The BBC B also requires a terminal emulator ROM.

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Southampton SO1 1LU.
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Telex: 477389 FLIGHT G
Fax: (0703) 330039 (3654:7:F)

Versatile interface for BBC computers

CONNECT3 is an interface for the BBC model B, B+ and Master computers ideally suited to a wide range of computer control and monitoring. It plugs into the user port and printer port of any suitable computer in the BBC family. It has its own mains powered supply.

Eight LEDs on the interface show the condition of the eight bits of the printer port. Two green, two yellow and four red LEDs are fitted, which help with traffic light simulation, for instance.

The eight printer port bits are buffered and switch power to eight 4 mm output sockets, providing up to 1 Amp at a voltage selected by a master switch. The supply voltage can be switched between 3, 4.5, 6, 9 and 12 Volts. The outputs can directly drive motors, lamps, relays and buzzers.

Forward, reverse, on and off control of motors is provided by four pairs of 'motor output' sockets. Printer port bit 0 is used to switch power to the first pair, and bit 1 drives an internal changeover relay to reverse the polarity. Bits 2 and 3, 4 and 5, and 6 and 7 are similarly paired. Four motors can be controlled in this way. For example, the motors for construction kits such as LEGO, Fischer Technic and Robotix kits can be connected direct to CONNECT3.

Eight buffered input sockets give access to the eight bits of the user port. Inputs can come from anything that closes a pair of contacts or switches a transistor on.

Four sockets provide earth return points for inputs and outputs, and a $+V_{out}$ socket provides a connection to the DC power supply. Connection to the outside world is by colour coded standard 4 mm jack sockets. A range of accessories is available with stackable matching plugs.

CONNECT3 is compatible with a range of control software available to schools, including JAVELIN, BITS, CONTROL-IT, and CONTROLLER. It can also be driven from Basic programs by writing to the printer port at address &FE61 and reading from the user port at &FE60. Software control of motor speed is possible using CONTROL-IT, or timer driven assembler code.

CONNECT3 costs £75.00 ex VAT.

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EW PRODUCTS • NEW PRODUCTS • NEW

The Protel PCB Design Package

An enhanced version of the popular low-cost PCB design package—Protel-PCB—is now available from UK distributor Engineering Solutions Limited.

Version 3.0, priced at £799.00, features netlist capability from compatible schematic software, Track/Layer swapping, additional text sizes, power and ground planes, NC drill support and EGA support for 640 × 350 pixel display.

Protel-PCB will design PCBs as large as 32 × 19 inches on six track layers to a one-thou grid resolution and additionally offers a range of features normally found only on expensive workstation design systems.

Other features include four track widths, six pad sizes, four edge connector pad sizes and two DIP pad sizes to suit a wide variety of applications.

The program generates multi-coloured checkplots, camera-ready artwork, Epson check printout and Gerber-compatible files, in addition to NC drill support.

A fully interactive evaluation disk is available from Engineering Solutions for 25.00.

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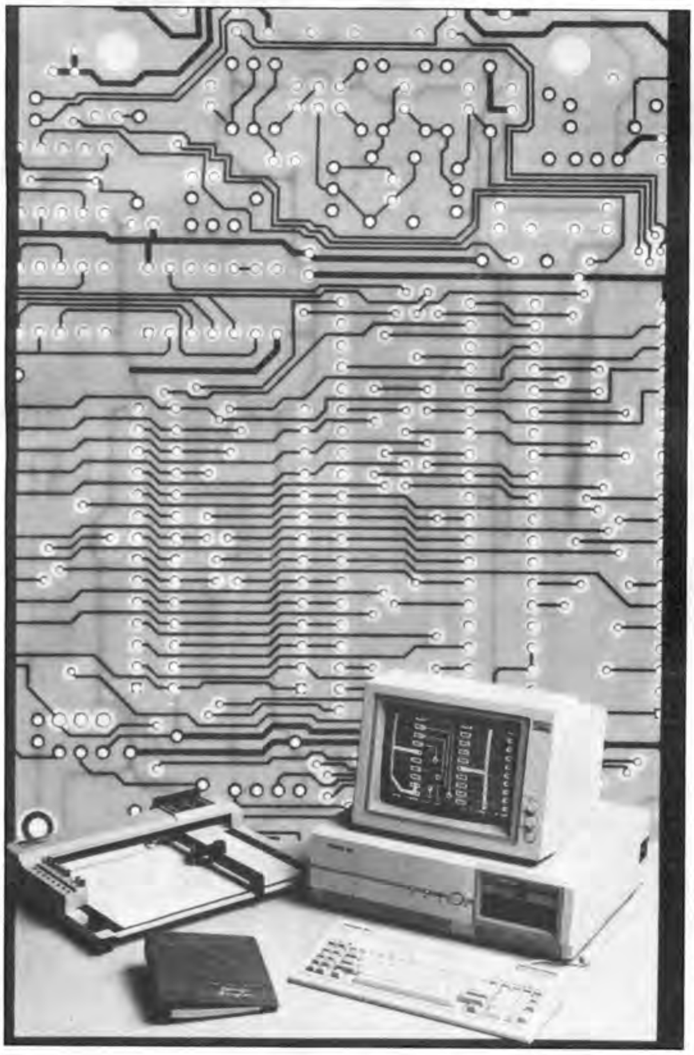
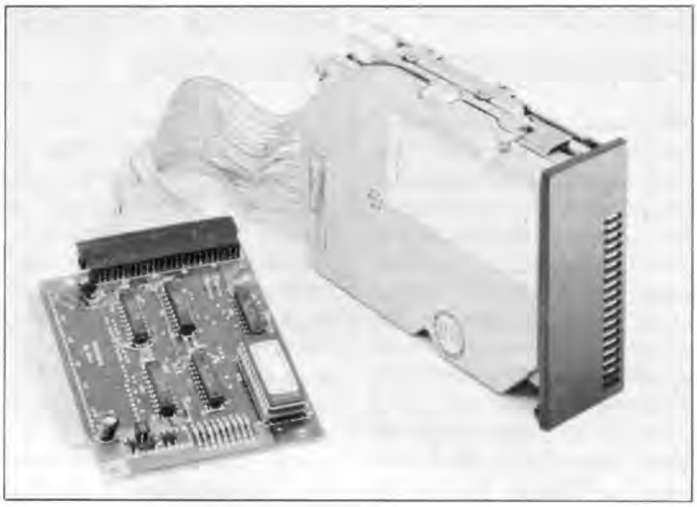


New 3½ inch hard disk drives



Epson (UK) Limited OEM Division have announced new 3½" disk-drives, the HMD 725A and HMD 726A. These bring Epson's 3½" range to three products and mark it as a major supplier to the burgeoning IBM Compatible hardware market-place.

The HMD 725A 21.4MB HDD comes with an interface card which plugs straight in to any IBM Compatible PC or XT and offers a highly cost effective hard disk option for both OEM's and dealers. The HMD 726A has an embedded SCSI interface and its different capacity makes it ideal for small system applications. Average access time of both units is 80 ms and they have a power consumption of 10 W.

Resident in the range is the HMD 720 with 20 MB of storage 69 ms average access time and a very low consumption of 8 W.

The HMD 725A and 26A units are available for volume delivery from April. All Epson hard drive products have a 20,000 POH MTBF reliability.

Epson OEM Division Manager Peter Gee adds: "These 2 new hard drives allow Epson to meet the demand expected from the industry as it ramps up to the future 3½" disk standard for all new generation PC's".

Epson (UK) Ltd is the UK market leader in printers and volume lap-top computers and is now the fourth largest supplier of IBM-compatible PC's. Additionally, the Company has a substantial computer-based components division. Epson (UK) Limited is a member of the Seiko-Epson Corporation.

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(3654:11:F)

New range of terminal block PCB connectors

Components and Electronics Limited, the new Surrey based connector supplier, announces the introduction of a new range of low cost modular terminal block connectors. Designed for use with PCBs, it is made up of 2, 3 and 4 way modules.

The board mounting receptacles can be supplies with either straight or right-angled terminations. Positive latching of plug to receptacle is incorporated as well as polarisation. These modules can be stacked to give the required connector size and are available in red or green to enable colour coding. These robust products should have many applications in the Electronic and Electrical Engineering Industries.

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Telephone: (0428) 54141.
(3654:6:F)

Fast optically-coupled sensor

Selectronic, the Witney-based optoelectronics specialist, now has a low-cost high-speed optical position sensing switch.

This infra-red device, designated LTH-301, is of the slot type, producing an output signal when the airgap between the emitter and sensor is obstructed by a projection on a rotating component or end of reel application. At 20 mA forward current and a 50% duty cycle, a typical risetime of 10 microseconds is claimed.

The device will switch voltages of up to 30 V, with a leakage current (dark) of less than 100 nA at 5 V. The current transfer ratio in a typical TTL-level application an 20 mA input current is 10%.

The switch is housed in a moulded plastic body with a 5.2 mm (0.2") airgap; it is compatible with DIL socket pin spacing. The operating temperature range is wide for a plastic encapsulation, being from −55 to +100 °C. The devices are 100% tested during manufacture, giving a claimed life in excess of 10,000 hours continuous use.

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Getting to grips with SMDs

Surface Mounted Devices (SMDs) are the latest stage in the evolution of printed board technology. Fused directly to the board, SMDs provide a completely reliable miniature connection resulting in a finished product far more compact than previously possible.

Toolrange are leaders in the field of providing state-of-the-art tools for the electronics industry. It is natural, therefore, that Toolrange should be the first to offer a product package specifically designed for use in SMD fabrication.

The Ersa SMD 1500 has been specifically developed for surface mount re-working and features a unique hand held tweezer tool that allows components to be gripped and heated simultaneously.

The unit comprises an electronic station, desoldering tweezers and a holder. Full temperature adjustment is provided by a rotary potentiometer from 70 °C to 400 °C. Each tweezer leg has a 6 watt rating and a set of angled desoldering tips to give access to difficult areas are supplied as standard.

The SMD 1500 has a zero potential connection so that a wide variety of SMD castings such as MELFs, mini mold chips and SO-8's can be re-worked in perfect safety.

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New Digital Multimeter

G80 is the latest digital multimeter from TMK instruments and is hardly larger than a credit card, making it easy to carry as well as easy to handle and easy to use. This 3½ digit LCD instrument has hundreds of general purpose applications in Industry, Education, Hobby and the Home. Full autoranging selects the correct range to give the best resolution for the test in hand, change the test value and the range will, if necessary, change to give the best answer.

Measurements are AC and DC volts from 1 mV to 450 V, with an input impedance of greater than 10 Mohms; Resistance from approximately 1 ohm to 20 Mohms; Audible and visual Continuity and a Diode Check. Other useful features include automatic indication on the 1999 count display of: Overrange, Polarity, Units of measurement and a warning of Low Battery. For just the recommended price of £24.95 the G80 comes complete in its own plastic wallet with instructions, test leads permanently attached, two 1.5 V batteries fitted ready for use and the price can put a G80 in everyone's pocket.

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(3654:10:F)

FILTERS: THEORY & PRACTICE — 2

by A.B. Bradshaw

Fundamental sections from which more complex ones are built are called **prototype filters**. The majority of filters used are **high-pass**, **low-pass**, **band-pass**, or **band-stop**. All of these are usually made up of low-loss reactances connected in **T**, π, or **L** form as shown in Fig. 1. Practical filters are normally designed as a combination of these configurations. In the following, the **reactance**, i.e., the imaginary part of a complex impedance, is designated by $\boldsymbol{X}$, which is equal to $1/\omega\boldsymbol{C}$ or $\omega\boldsymbol{L}$ or a combination of these.

Low-pass filters

In a correctly terminated low-pass T filter, see Fig. 15:

$$Z_{0T} = \sqrt{Z_1\,Z_2 + Z_1^2/4} =$$

$$\sqrt{jX_1\,jX_2 - X_1^2/4}$$

which can also be expressed as

$$Z_{0T} = j\sqrt{X_1\,(X_1/4 + X_2)} \qquad [20]$$

If X_1 and $(X_1/4+X_2)$ are of **opposite** sign, Z_{0T} is resistive and the filter draws power: it is operating in its **pass-band**—see Fig. 17.

If X_1 and $(X_1/4+X_2)$ are of the **same** sign, Z_{0T} is reactive and the filter reflects power: it is operating in its **stop-band**—see Fig. 17.

In a low-pass π filter—see Fig. 16, Z_{0T} and $Z_{0\pi}$ are related by

$$Z_{0\pi} = \frac{Z_1Z_2}{Z_{0T}} = \frac{jX_1X_2}{j\sqrt{X_1(X_1/4+X_2)}}$$

$$= \frac{j^2X_1X_2}{Z_{0T}} = \frac{-X_1X_2}{Z_{0T}} \qquad [21]$$

Since X_1 and X_2 are of opposite sign, their product is a constant, so that

$$Z_{0\pi} = \frac{\text{CONSTANT}}{Z_{0T}} \qquad [22]$$

in which Z_{0T} varies as in the previous example—see Fig. 17. The value of f_c may be determined from an inspection of the characteristics in Fig. 17, but can also be evaluated from Eq. [19]:

$$\cosh\gamma = 1 + \frac{Z_1}{2Z_2}$$

For the T section,

$$\cosh\gamma = 1 - \frac{\omega^2LC}{2}$$

but since $\gamma = \alpha + j\beta$,

$$\cosh(\alpha + j\beta) = \cosh\alpha\cosh j\beta + \sinh\alpha\sinh j\beta \qquad [23]$$

Since, $\cosh j\beta = \cos\beta$
and $\sinh j\beta = j\sin\beta$
Eq. [23] becomes

$$\cosh\alpha\cos\beta + j\sinh\alpha\sin\beta =$$

$$1 - \frac{\omega^2LC}{2} \qquad [24]$$

Since the right-hand term in [24] does not contain an imaginary part, the expression can be split into

$$\cosh\alpha\cos\beta = 1 - \frac{\omega^2LC}{2}\ \text{(real part)}$$

and

$$\sin\alpha\sin\beta = 0\ \text{(imaginary part)}$$

Considering the real part, in the pass-band the attenuation is zero, so that $\alpha = 0$, and

$$\cos\beta = 1 - \frac{\omega^2LC}{2} \qquad [25]$$

Inserting the two maximum values of a cosine curve, i.e., ±1, in this expression yields

$$+1 = 1 - \frac{\omega^2LC}{2}$$

and

$$-1 = 1 - \frac{\omega^2LC}{2}$$

From these, the two cut-off frequencies can be determined:

$$f_1 = 0\ \text{Hz} \qquad [26a]$$

and

$$f_c = \frac{1}{\pi\sqrt{LC}} \qquad [26b]$$

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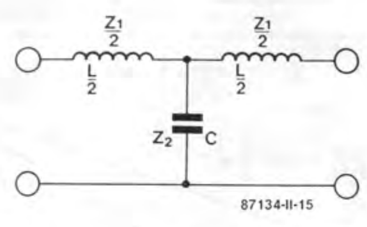

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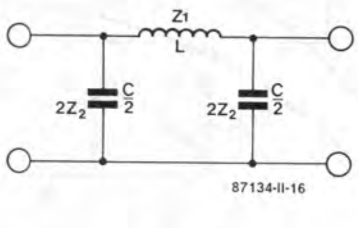

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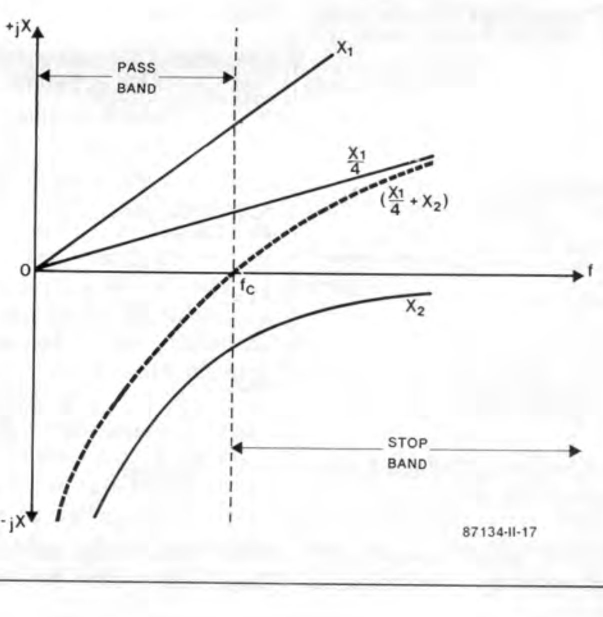

The phase angle, β, can be found by inserting the value of f_c [26b] into [25] to give

$$\cos\beta = 1 - 2(f/f_c)^2$$

so that

$$\beta = \cos^{-1}[1 - 2(f/f_c)^2] \text{ radians} \quad [27]$$

Expression [27] is shown diagrammatically in Fig. 18.
In the stop band $\beta = \pi$, so that $\cos\beta = -1$. Inserting this in [24a] gives

$$\cosh\alpha = \frac{\omega^2 LC}{2} - 1$$

so that

$$\alpha = \cosh^{-1}[2\,(f/f_c)^2 - 1] \text{ nepers} \quad [28]$$

where α is the attenuation in the stop band. This expression is shown graphically in Fig. 19.
In a low-pass T filter, $Z_1 = j\omega L$ and $Z_2 = 1/j\omega C$, so that $Z_1Z_2 = L/C$. Inserting this in Eq. [5] gives

$$Z_{0T} = \sqrt{\frac{L}{C} - \frac{\omega^2 L^2}{4}} \quad [29]$$

When $f=0$,

$$Z_{0T} = \sqrt{L/C}$$

When $f=f_c$,

$$Z_{0T} = \sqrt{\frac{L}{C} - \frac{L}{C}} = 0$$

Therefore, over the pass-band from $f=0$ to $f=f_c$, Z_{0T} moves from $\sqrt{L/C}$ to zero ohms.
Since the π network is related to the T type, it may be concluded that

$$Z_{0\pi} = \frac{Z_1 Z_2}{Z_{0T}} = \frac{L/C}{\sqrt{L/C - \omega^2 L^2/4}} \quad [30]$$

When $f=0$,

$$Z_{0\pi} = \sqrt{L/C}$$

When $f=f_c$,

$$Z_{0\pi} = \frac{L/C}{\sqrt{L/C - L/C}} = \infty$$

The variations of Z_{0T} and $Z_{0\pi}$ are shown in Fig. 20.

The basic design equations can be obtained from the foregoing discussions, but are summarized here for convenience's sake: they apply to T and π sections alike.

$$Z_0 = R_0 = \sqrt{L/C}$$

$$f_c = 1/\sqrt{LC}$$

$$L = C R_0^2$$

$$C = 1/\pi R_0 f_c$$

High-pass filters

In similar vein as the considerations on the low-pass filters, the reactances and impedances in a high-pass T filter as shown in Fig. 21 are

$$X_1 = 1/\omega C \text{ or } Z_1 = 1/j\omega C$$

and

$$X_2 = \omega L \text{ or } Z_2 = j\omega L$$

so that

$$X_1/4 + X_2 = \omega L - 1/4\omega C$$

A graphical representation of these reactances is shown in Fig. 22.
Substituting the impedance values given above into Eq. [19] yields

$$\cosh\gamma = 1 - \frac{1}{2\omega^2 LC}$$

By a similar consideration as before,

$$\cosh\alpha\cos\beta = 1 - \frac{1}{2\omega^2 LC}$$

In the pass-band, $\alpha = 0$, so that $\cosh\alpha = 1$, and

$$\cos\beta = 1 - \frac{1}{2\omega^2 LC} \quad [31]$$

Substituting the limits of ±1 for $\cos\beta$ in [31] gives

$$+1 = 1 - \frac{1}{2\omega^2 LC}$$

and

$$-1 = 1 - \frac{1}{2\omega^2 LC}$$

From these values the cut-off frequencies can be deter-

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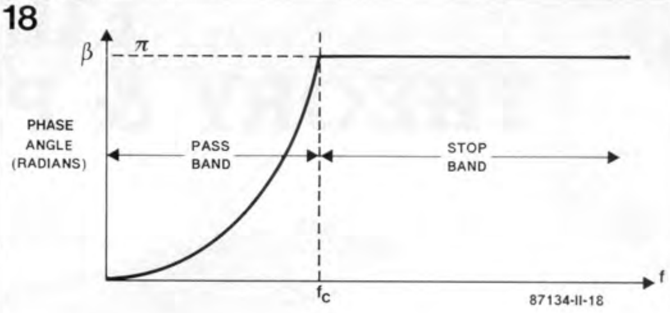

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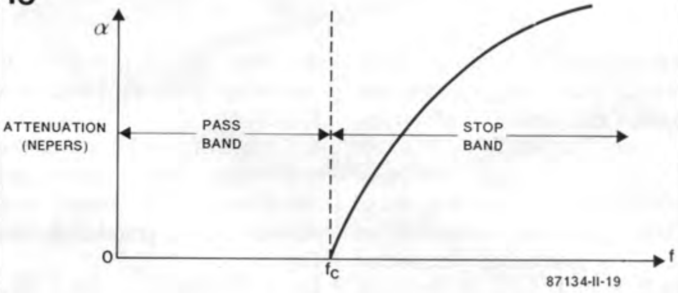

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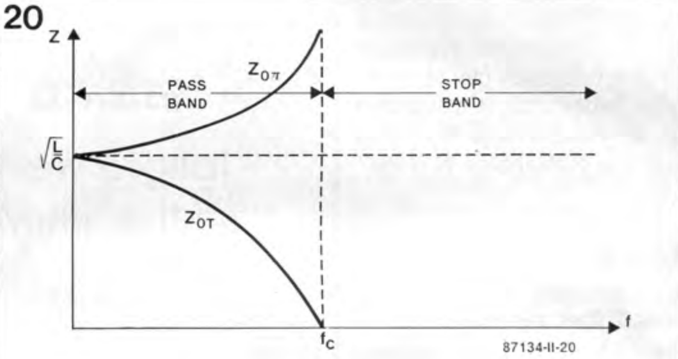

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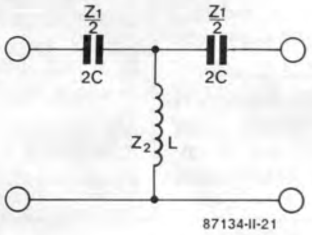

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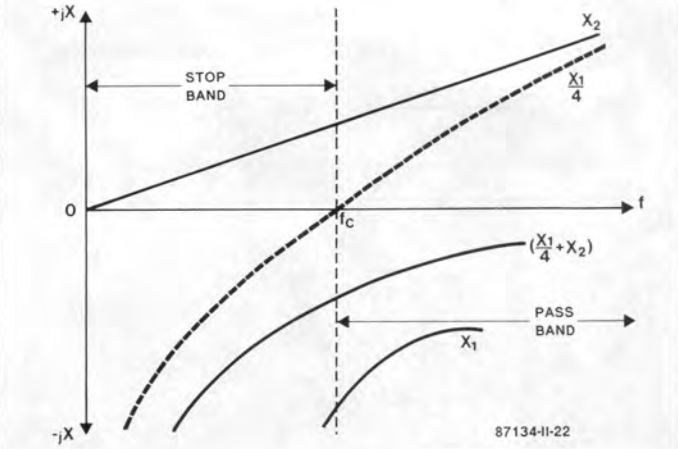

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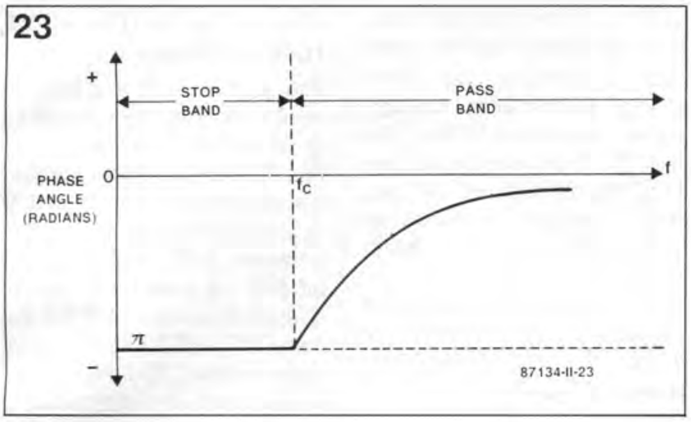

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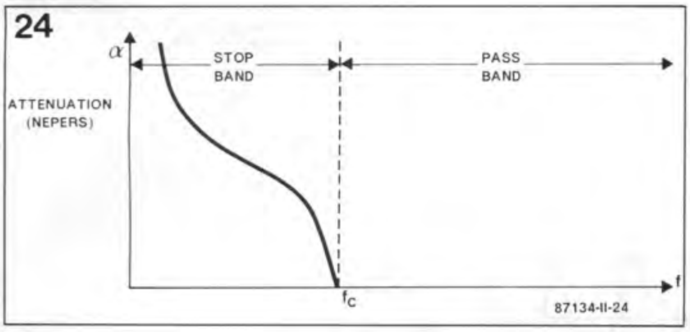

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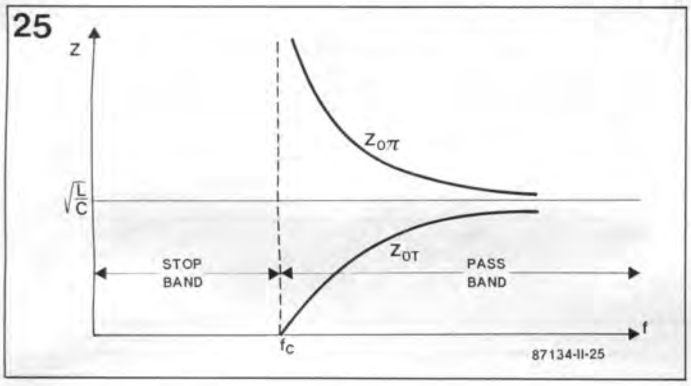

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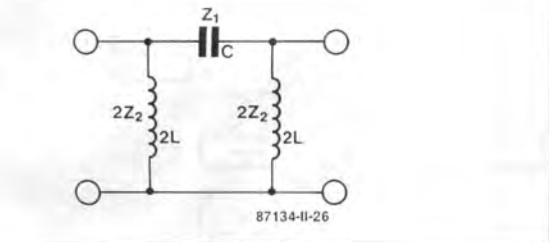

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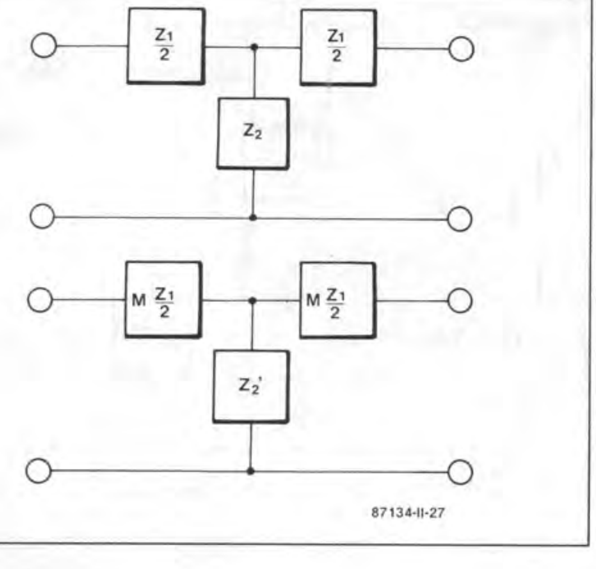

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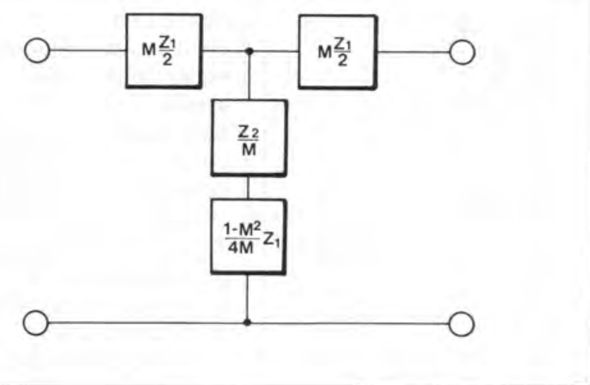

mined:

$$f_c = \frac{1}{4\pi\sqrt{LC}} \qquad [32a]$$

and

$$f_1 = \infty \qquad [32b]$$

The phase angle, β, is given by

$$\beta = \cos^{-1}[1 - 2(f/f_c^2] \text{ radians} \qquad [33]$$

The phase angle characteristic is shown in Fig.23, from which it is seen that $\beta = -\pi$ over the stop band and reduces to zero in the pass band.
Similarly,

$$\alpha = \cosh^{-1}[2(f_c/f)^2 - 1] \text{ nepers} \qquad [34]$$

The attenuation characteristic is given in Fig. 24.
The impedance variation in a high-pass T filter is calculated with Eq. [5]:
when $f = \infty$,

$$Z_{0T} = \sqrt{L/C} \qquad [35a]$$

and when $f = f_c$,

$$Z_{0T} = 0 \qquad [35b]$$

The impedance characteristic is shown in Fig. 25.
The component values can be calculated with the aid of Eq. 32 and Eq. 35.
Eq. [19] applies to the high-pass π filter shown in Fig. 26: the phase angle and attenuation characteristics of this type of filter are the same as those of a T type and are determined by applying the procedures outlined before.
The filters discussed so far are often referred to as "constant-*k*" types because $Z_1Z_2 = L/C$, which is independent of ω. Although constant-*k* sections are useful for simple filtering requirements, they have two serious shortcomings:

(a) Z_0 varies over the pass band which can cause mismatch; and

(b) α rises only slowly outside the pass band.

Typical figures in a low-pass constant-*k* section are a 10 dB increase in attenuation at 1.2 f_c and $Z_0 = 2.3R_0$ at $f = 0.9f_c$. Clearly, what is needed is a constant Z_0 in the pass band and a far more rapid rise in attenuation outside the pass band. These requirements are approached in *M*-derived filters.

M-derived filters

Figure 27 shows two low-pass T sections, of which that in 27a has series impedances as discussed before, while that in 27b has series impedances that have been modified by a factor *M*. This factor is an undefined constant (whose numerical value lies between zero and unity), which has given rise to the name "*M*-derived".
For the constant-*k* section

$$Z_{0T} = \sqrt{Z_1Z_2 + Z_1^2/4} \qquad [5]$$

while for the *M*-derived section

$$Z_{0TM} = \sqrt{MZ_1Z_2 + M^2Z_1^2/4} \qquad [36]$$

These impedances will be equal if

$$Z_2' = \frac{Z_2}{M} + Z_1\frac{1-M^2}{4M}$$

With this result, Fig. 27b is redrawn as shown in Fig. 28. It is seen that the centre limb is made up of the opposite kinds of impedance in series, i.e., a

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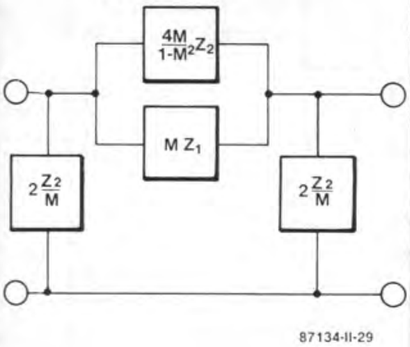

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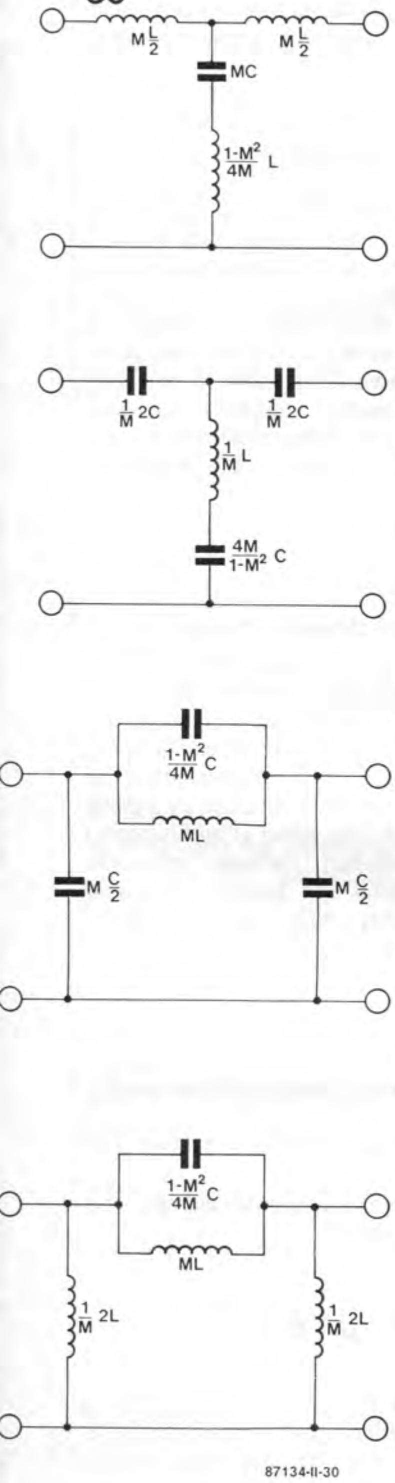

tuned circuit, where all values depend on *M*.

By the same type of equivalence, the *M*-derived π section shown in Fig. 29 is obtained. Here again, the centre limb consists of opposite impedances, which form a parallel-tuned circuit.

The constant-*k* low-pass and high-pass sections of Fig. 15, 16, 21 and 26 are modified to *M*-derived sections in Fig. 30.

It should be appreciated that series or parallel resonance can occur in these *M*-derived sections. This aspect makes it possible to improve the rather sloppy performance of constant-*k* prototypes. None the less, the good attenuation performance far outside the pass band exhibited in constant-*k* sections will still be of value in combination filters.

The attenuation vs frequency characteristics with values of 0.3, 0.6, 0.8, and 0.9 for *M* are shown in Fig. 31.

M-derived terminating half sections

The asymmetrical T/2 and π/2 sections of Fig. 11 are modified to *M*-derived half sections in Fig. 32. The usefulness of these terminating sections is that if *M* is given a value of 0.6, Z_0 lies between $0.9Z_0$ and $1.1Z_0$ for most of the pass band. Consequently, this value of *M* has become the standard for terminating sections. The variation of Z_0 as a function of frequency is

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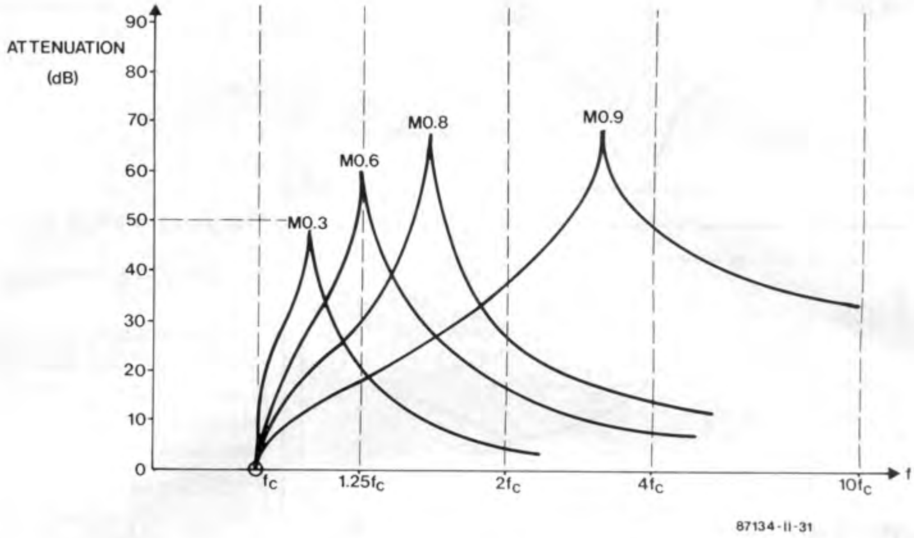

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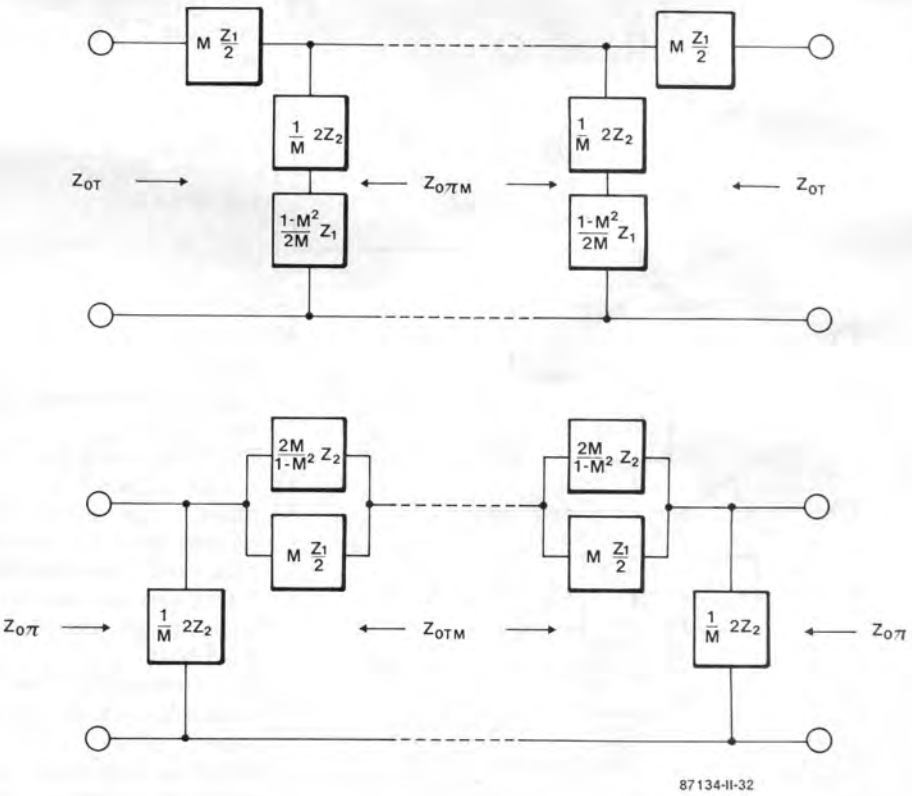

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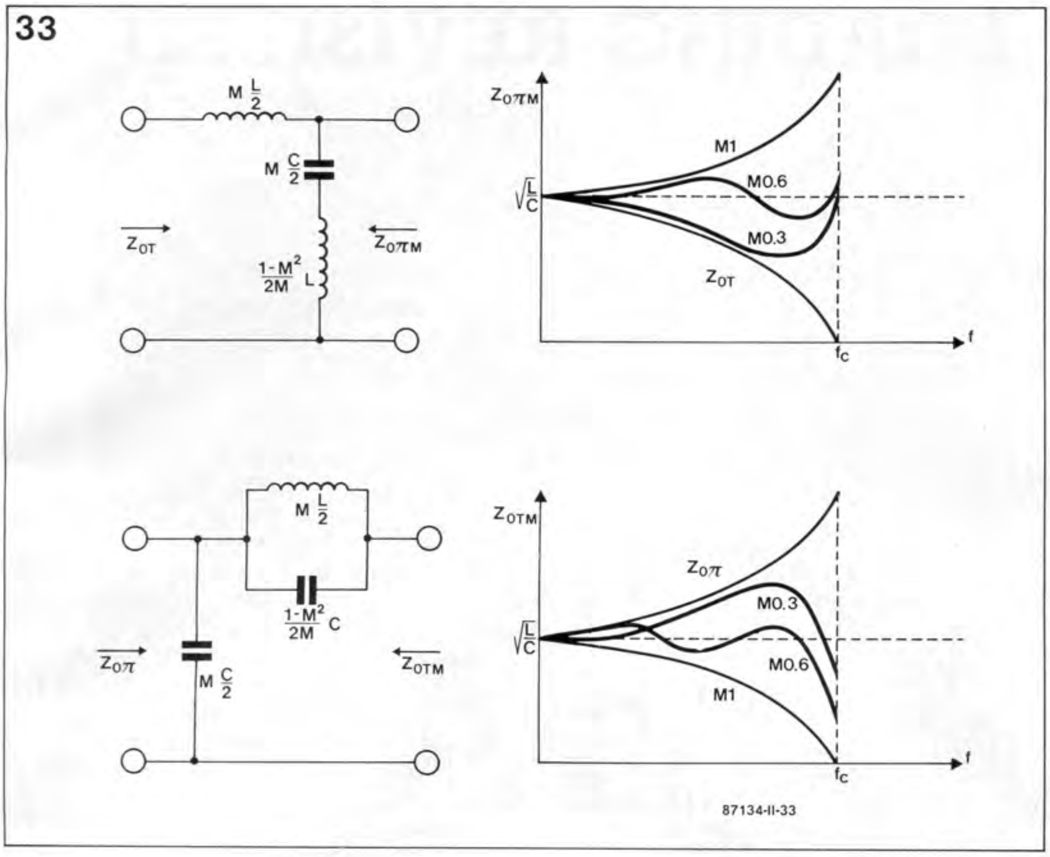

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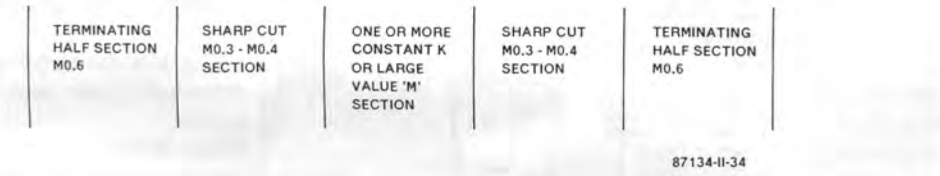
TERMINATING HALF SECTION M0.6
SHARP CUT M0.3 - M0.4 SECTION
ONE OR MORE CONSTANT K OR LARGE VALUE 'M' SECTION
SHARP CUT M0.3 - M0.4 SECTION
TERMINATING HALF SECTION M0.6
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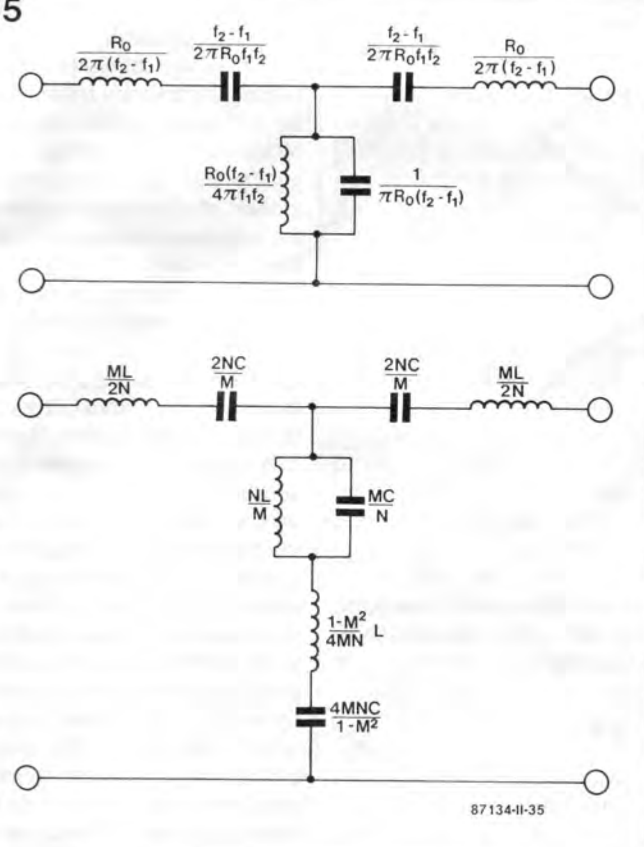

shown in Fig. 33 for both a T and a π half section.

Low-pass and high-pass filters are designed to a given specification by combining *M*-derived terminating sections with small-value *M* sections, and either constant-*k* or large-value *M* sections in the middle so that the attenuation far from the cut-off frequency can be made large. A typical cascade is shown in Fig. 34.

The foregoing covers the basic principles of the **image parameter network theory.** Band-pass filters, both constant-*k* and *M*-derived, can be designed with the aid of this theory, but the computations tend to become cumbersome. Band-pass filters may be constructed by cascading low-pass and high-pass sections, particularly when large bandwidths are required, but this method presents difficulties with true band-pass designs. None the less, design equations for a constant-*k* and an *M*-derived band-pass filter as shown in Fig. 35 are given here without proof:

$$f_{1\infty} f_{2\infty} = f_0^2$$

$$f_{2\infty} - f_{1\infty} = 2Nf_0/\sqrt{(1-M^2)} =$$

$$\frac{\text{bandwidth}}{\sqrt{(1-M^2)}}$$

In modern network theory (synthesis techniques), tables are available that enable the design of low-pass, high-pass, and band-pass filters from AF up to about 500 MHz to be undertaken with the aid of a hand-held calculator only.

The concluding part of this article will be published in next month's issue.

RADIO AMATEURS' COURSES

The North Trafford College is offering more courses for radio amateurs starting this month. The courses comprise

- THEORY on Monday or Thursday evenings or on Wednesday mornings:
- MORSE CODE on Tuesday evenings or on Wednesday afternoons;
- ADVANCED MORSE CODE on Monday evenings.

The college also offers a number of courses on electronics servicing and radio, television, and video recorder servicing.

It should be noted that unemployed persons can attend the college for a maximum of twenty-one hours each week and still receive full unemployment benefit.

Enrolment is on 2, 3, and 4 September 1987.

Full details can be obtained from:

J.T. Beaumont, G3NGD
North Trafford College of F.E.
Talbot Road
Stretford
MANCHESTER M32 0XH
Telephone: 061 872 3731
Ext 45

HORN LOADING REVISITED

by R.M. Harris, B.Sc.

Horn loudspeakers provide good low-frequency performance and high efficiency, but are impractical for many uses because they are very large. However, R.M. Harris describes a design that is suitable for use in an ordinary living room.

The weakest link in any hi-fi system is undoubtedly the acoustical transducer or loudspeaker. Sound recording technology is reaching new levels of precision and noise reduction with digital recording and compact discs. Amplifiers can be perfected to almost any degree, if the price is right, with hitherto unheard of purity in terms of harmonic distortion and intermodulation products. In other words, it is possible to reproduce sound faithfully from DC to RF, but only in terms of **electrical signals**. For, while electronic technology has passed from thermionic valves through discrete transistors to integrated circuits, the loudspeaker has hardly changed in its essentials since its invention in 1925*.

Since middle- and high-frequency propagation is characterized by small-amplitude sound waves, which eases most engineering problems, this article is confined to the problem of obtaining good, clean low-frequency sound reproduction.

Two physical principles account for most of the engineering difficulties at low frequencies. The first is that for a plane propagating sound wave the pressure, p, and particle velocity, u, are related in terms of the specific acoustic impedance of the medium (air):

$$p/u = Z_o \qquad [1]$$

where

$$Z_o = \varrho_o c \qquad [2]$$

in which ϱ_o is the density of the medium and c is the velocity of sound in the medium.

At a point in space, the instantaneous particle displacement, y, of a sinusoidal sound wave of amplitude a and frequency f Hz, is given by

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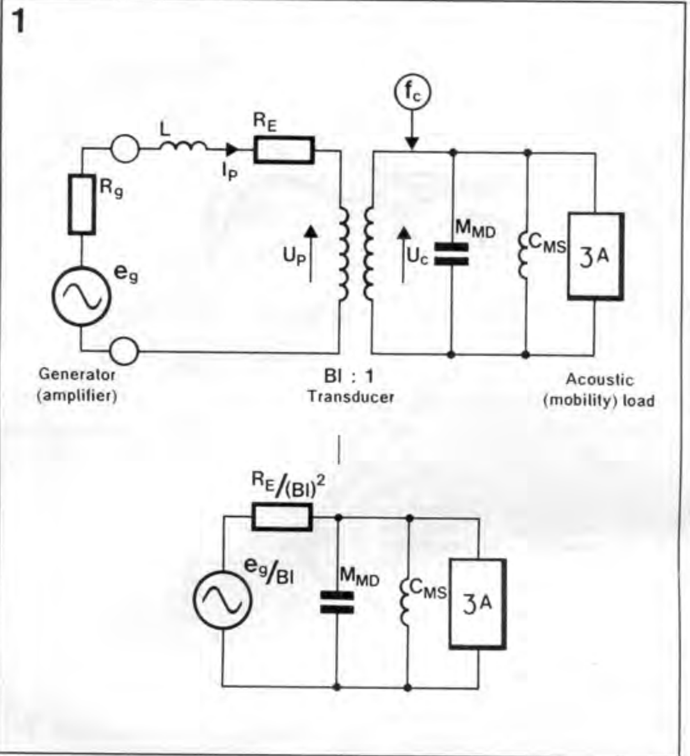

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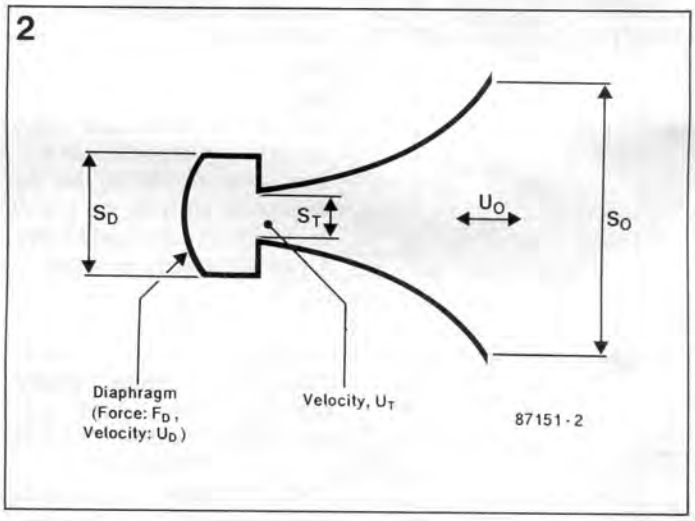

$$y = a\sin 2\pi ft \qquad [3]$$

and the instantaneous velocity is

$$u_t = dy/dt = 2\pi af\cos 2\pi ft \qquad [4]$$

and the maximum velocity is

$$u = 2\pi fa \qquad [5]$$

For a given sound pressure level—SPL—of p, the amplitude is given by

$$a = u/2\pi f \qquad [6]$$

$$= Z_o p/2\pi f \qquad [7]$$

Both [6] and [7] simply state that the amplitude increases as the frequency decreases.

The second principle is that at low frequencies the wavelength in air is much larger than the dimensions of the sound source. This results in the radiation of spherical wave fronts from what is, in effect, a point source. The specific acoustic impedance, Z_s, is not the same for diverging waves, as given by the general formula

$$Z_s = \frac{p}{u} = \frac{\varrho_o ckr}{\sqrt{1 + k^2 r^2}}\ 90° - \arctan kr \qquad [8]$$

where r is the radial distance from the point source, and $k = 2\pi/\lambda$.

When $kr >> 1$ ($r >> \lambda/2\pi$), the magnitude of Z_s approaches the value for a plane wave ($\varrho_o c$) with u in phase with p. For $k2 = 1$, Z_s goes to zero and u tends to be in phase quadrature with p. The real part of Z_s (which is generally complex) falls to zero as r^2, which means that the mismatch between the transducer and the medium degrades in direct proportion to the square of the wavelength.

The corollary is that the speaker cone has to execute larger movements to maintain a constant SPL at lower frequencies if Z_s remains constant. If, however, Z_s (and in particular the real part of Z_s) falls at lower frequencies, the situation is exacerbated. So, all effects included, the cone amplitude needs to vary as λ^3 or as f^{-3}.

The foregoing general analysis clinches the central problem of designing for efficient bass reproduction. Large amplitudes are deprecated for moving-coil driver units: they introduce not only mechanical difficulties, but also distortion. It has been stated (Ref. 1) that any movement of the cone entails some distortion: the more it moves,

the worse the distortion. Unfortunately, the ear is adept at sensing very low levels of distortion, especially intermodulation distortion.

The concept of transforming electrical energy into acoustic energy introduces ideas of impedance matching and transducers. Without going into the intricacies of acoustics theory, the following simplified treatment of the method of "electrical analogy" may be helpful. The complete sound reproduction system from amplifier to air can be represented by an electrical equivalent circuit—see Fig. la. The constant-voltage generator has an internal resistance, R_g, which is typically 0.2Ω for modern amplifiers. The voice coil of the driver unit contributes inductance, L, and pure resistance, R. The essential function of the driver unit is that of energy transducer, which can be represented as a transformer with a turns ratio of Bl:1. The primary current, I_P, gives rise to a force f_P which, as it were, flows in the secondary circuit. The voltage induced back across the primary, V_P, reflects the velocity, u_C, of the voice coil. Thus, $I_P=f_C/Bl$ and $V_P=Blu_C$.

The primary impedance, Z_1, is related to the secondary impedance, Z_2, as follows

$$Z_1 = V_P/I_P$$

and

$$Z_2 = u_C/f_C$$

so that

$$Z_1 = (Bl)^2 Z_2 \qquad [9]$$

The term Bl is the magnetomotive force factor, which is measured in tesla per metre (T m^{-1}).

Note that in the secondary circuit impedance is the inverse of the better known mechanical analogue where voltage corresponds to force and current to velocity. In the present system, known as the mobility system (Ref. 2), inertia becomes a shunt capacitance and spring resistance becomes a shunt inductance. Hence, the moving mass of the speaker is represented by capacitance M_{MD}, while the stiffness of the suspension and any enclosed volume (e.g. in infinite baffle designs) of air are represented jointly by inductance C_{MS}. The acoustic load is represented by $_A$, the acoustic mobility, which is the reciprocal of acoustic impedance.

For maximum energy transfer, the blocking effects of the mechanical inertia and stiffness have to be minimized. In the mobility system, this amounts to reducing the magnitude of ß$_{-A}$ (particularly the real part) below the shunt admittances of M_{MD} and C_{MS}. Then, ß$_{-A}$ will predominate in the secondary load.

The accompanying step is to reduce the size of the primary series impedances as reflected in the secondary—see Fig. lb. At low frequencies, L may be disregarded. Considering the difficulty of achieving large enough values of acoustic impedance (i.e., low enough values of acoustic mobility, ß$_{-A}$), every effort has to be made to reduce the moving mass and stiffness of the suspension. Furthermore, Bl needs to be maximized to minimize the dissipative effect of R_E. The closed cabinet or infinite baffle design reduces stiffness by the use of a large enclosed volume, increases Z_A by the use of a large cone, and then fails to reduce the moving mass (which includes a cylinder of air in front of the cone that is about a third of the cone radius deep). Such designs seldom achieve energy efficiencies much above 4%, in spite of decades of research.

The horn as an acoustical transformer

For a sound wave propagating along an exponential horn, the particle velocity and pressure vary in proportion to the diameter of the horn. The specific acoustic impedance

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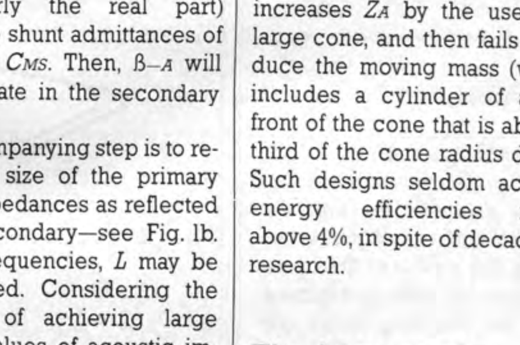

therefore remains constant. On the other hand, the acoustic impedance is defined as the pressure divided by the flow (=velocity times cross-sectional area). So, in the exponential horn, acoustic impedance varies inversely as the cross-sectional area. The horn transforms a small flow at high pressure in the throat to a large flow at low pressure in the mouth. Conventionally, the horn is driven by a diaphragm (e.g., the cone of a loudspeaker) of larger cross-sectional area, S_D, than that of the throat, S_T, as shown in Fig. 2. The force, F_D, acting on the diaphragm is related to the pressure, p_T, in the throat by:

$$F_D = S_D p_T \qquad [10]$$

Also,

$$u_D = u_T S_T / S_D \qquad [11]$$

where u_D is the velocity of the diaphragm and u_T is the particle velocity in the throat.

The mechanical impedance, Z_M, is defined as force per unit velocity. So, for the diaphragm,

$$Z_M = F_o / u_D$$

$$= (S_D^2 p_T)/(S_T u_T)$$

$$= (S_D^2/S_T)(p_o/u_o) \qquad [12]$$

where p_o and u_o are the pressure and velocity respectively in the mouth of the horn.

For a horn of sufficient dimensions, the coupling to the outside world becomes 100% and the specific acoustic impedance at the throat approaches $\varrho_o c$. Strictly, this is true only for an infinite horn, but for practical purposes a horn of which the circumference of its mouth equals the wavelength of the lowest frequency to be propagated is adequate. Under these conditions, the mechanical impedance becomes

$$Z_M \approx \varrho_o c(S_D^2/S_T) \qquad [13]$$

To equal this value of Z_M, an infinite baffle design would require a cone diameter of λ/π, where λ is the wavelength. At 40 Hz, $\lambda = 8.28$ m, resulting in an impractical cone of more than 2.5 m in diameter.

The most serious restriction relating to low-frequency applications of horns is the cut-off frequency, f_L, below which sound will not propagate. If the cross-sectional area of the horn varies with the distance, x, along the horn as

$$S_x = S_T \exp(mx) \qquad [14]$$

the parameter m, expressed in m^{-1}, is called the **flare** constant. The low-frequency cut-off is given by

$$f_L = mc/4\pi \qquad [15]$$

For instance, if $m = 0.3646\ m^{-1}$, $f_L = 40$ Hz.

For an infinite exponential horn, the real part of the throat impedance falls abruptly to zero at the cut-off frequency—see Fig. 3. The imaginary (reactive) part rises to a maximum at f_L and then falls asymptotically to zero. Above f_L it resembles a mirror image of normal capacitive reactance, which is the reason that it is often called negative capacitance reac-

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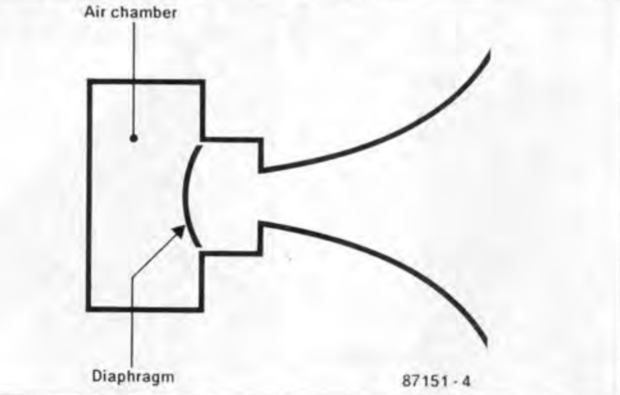

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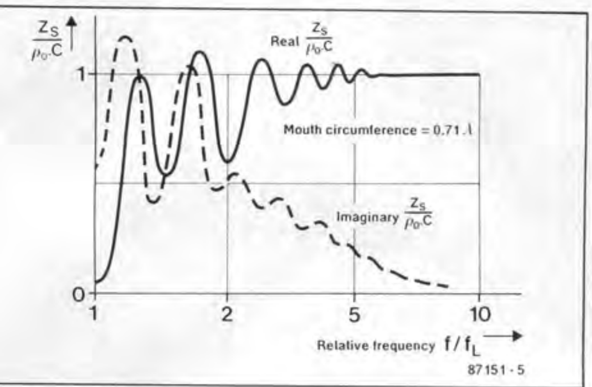

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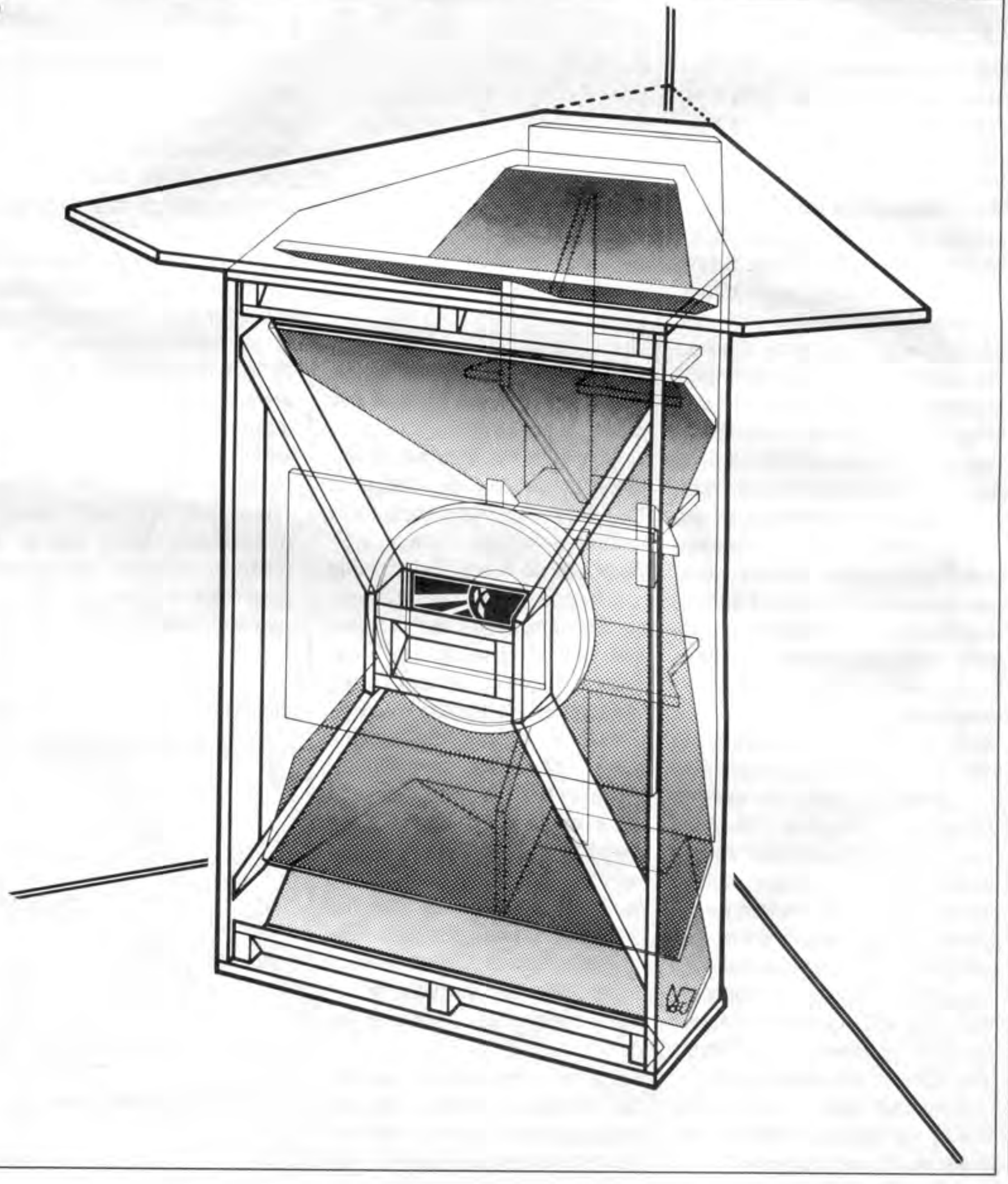

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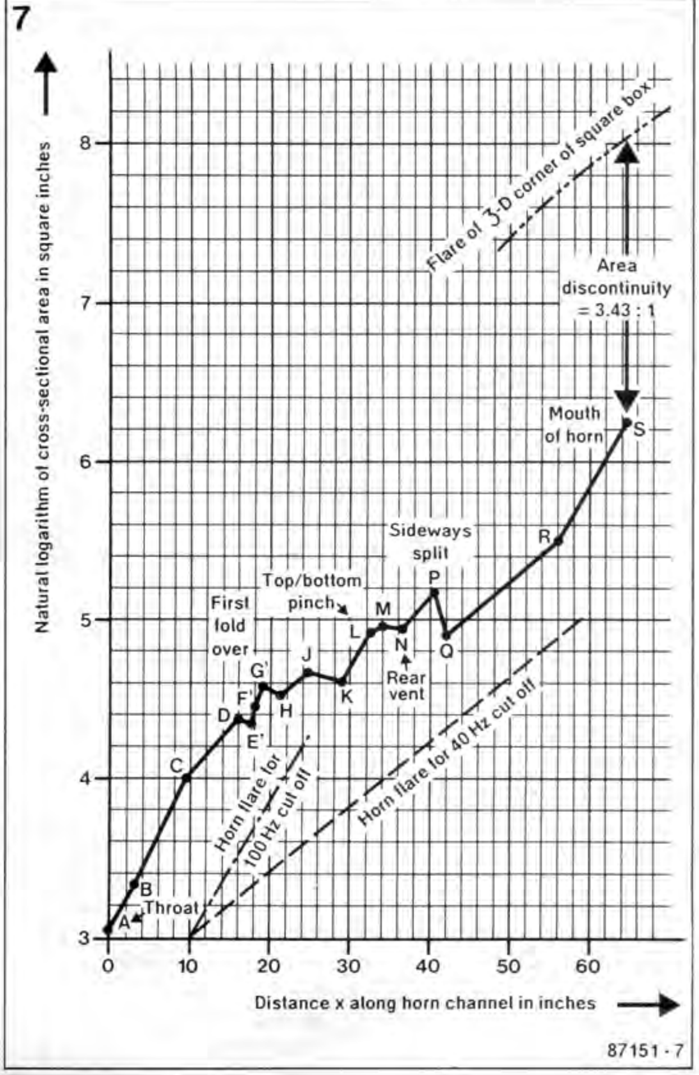

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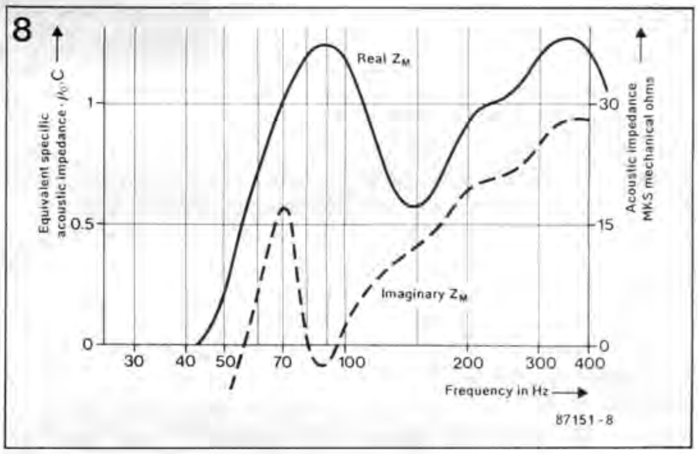

tance. It also indicates the way to compensate it, namely by the series connection of a positive capacitive reactance of the same magnitude. In acoustics terms, this amounts to placing a compliant volume of air behind the diaphragm, enclosed in an airtight chamber—see Fig. 4. Note that this action is not in any way a frequency-selective tuning operation: in principle, it is rather a broad-band reactance annulling process.

The volume of the air chamber is calculated by multiplying the throat area, S_T, by the length in which the horn doubles its cross-sectional area, and then by 2.9. Typically, this volume is small compared with the enclosed volumes required for infinite baffle designs.

For finite horns, the throat-impedance curves exhibit a degree of periodicity, with the depth of the oscillations increasing as the horn is made shorter and thinner. Fig. 5 shows the behaviour of the real and imaginary parts of the throat impedance, computed by Olson, for a horn with a mouth circumference of $0.71\lambda_L$, where λ_L is the wavelength at the cut-off frequency. Once the flare constant and the size of the mouth have been decided, the length of the horn depends only on the size of the throat. Often, the desirable length is quite impractical at low frequencies.

Practical constraints

Ideally, the horn would possess a wide mouth, say, 8.3 m circumference for good matching to the room at 40 Hz: this would entail a length of around 5 m. Some design compromise is clearly indicated if horn-loaded enclosures are to be adopted for semi-fixed or even portable applications. A number of actions can be taken to ease the dimensional limitations. The best-known of these is to fold the horn back onto itself once or twice to make a more compact, box-shaped structure. Less well-known, perhaps, is the method used by Lee in his catenoid design (Ref. 3), or that of P.W. Klipsch, in which the mouth of the horn is made to illuminate the room from one of its corners.

The effectiveness of the Klipsch method can be understood by considering the fact that placing a sound source close to a solid plane produces an in-phase image behind the plane. Similarly, a source located near the intersection of two planes gives rise to two images, and near a corner of a rectangular box three in-phase images accompany the source. The effect of placing the mouth of a horn near a corner is to quadruple the effective mouth area, which very usefully relaxes the earlier stated conditions on mouth circumference: it halves the circumference.

The klipschorn

P.W. Klipsch described a *Low Frequency Horn of Small Dimensions* (Ref. 4) in 1941. His experimental work was cut short by the Second World War, but provided enough data to establish the final design with confidence. It included all the design improvements described in the foregoing section in an ingeniously designed cabinet pictured in Fig. 6.

The design cleverly conceals a doubly split reflex horn of over 1.5 m in length, and makes use of the room walls for two sides of the horn. The mouth of the horn is formed by two rectangular, vertical slots (including the contiguous images in the walls and floor) which make a phased array that helps to beam sound in the horizontal plane, and at the same time increases the specific acoustic impedance.

I shall not repeat or even summarize Klipsch's detailed analysis, but rather assume his measured results and apply them to the present project, which consists of a klipschorn enclosure and a Richard Allen CG12 driver unit. Klipsch used a mains energized Jensen 12, 12-inch driver, which enabled some acoustical measurements to be made via the voice coil terminals simply by switching on or off the magnetic field. The wedge-shaped air chamber has a volume of 64 l of which 9.8 l were taken up by the driver unit.

The chamber, by virtue of its pyramidal shape, was free of mid-range resonances and required no damping (which would reduce efficiency in any case).

The piston diameter of the cone (10.5 in) gave an area $S_D=0.0558$ m^2, which was reduced to 0.0322 m^2 at the entrance to the throat to give a ratio $S_D/S_T=1.73$ in Eq. [11]. This was found to be too large at the lowest frequencies, and so a "rubber throat" was devised to give an effective throat area of 0.0644 m^2 at 40 Hz, reducing to 0.0322 m^2 at 100 Hz. The "rubber throat" was brought about by making the first section of the multi-flared horn cut off at 100 Hz, and the rest of the horn at 40 Hz.

The throat opened into a split horn with symmetrical channels pointing up and down for the 100 Hz cut-off section. The two channels folded around the top and bottom of the air chamber, constricting in the lateral dimension, but flaring in the vertical.

The 40 Hz cut-off flare constant was approximately maintained with the aid of a succession of short linear flares for ease of construction.

The sharp corner of the room was hidden by a fillet plate which deflected the now merged sound from upper and lower channels sideways between cabinet sides and walls.

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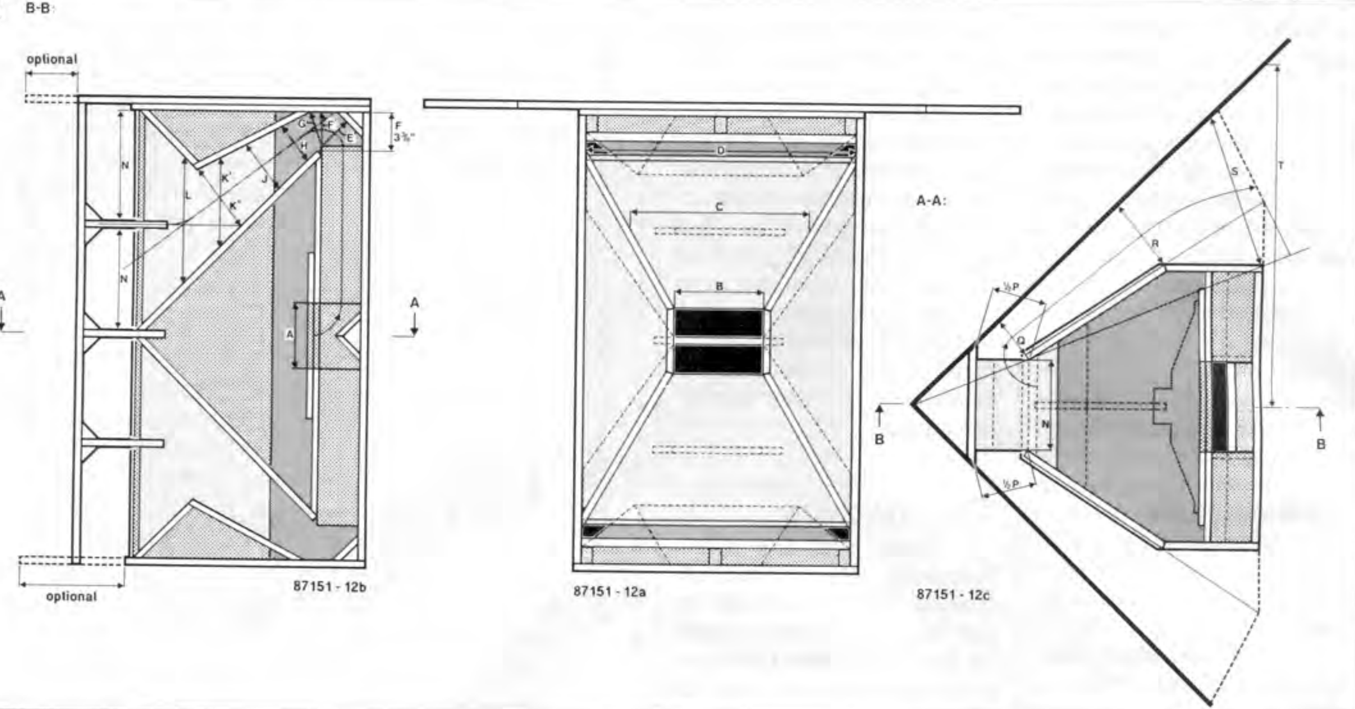

This time, the horn was split laterally and symmetrically if the cabinet was placed correctly. Fig. 7 shows the multi-flared profile, where the natural logarithm of the cross-sectional area has been plotted against channel distance.

Calculated performance with a Richard Allen CG12 driver

Klipsch measured the acoustic impedance, Z_T, of the horn channel with and without the air chamber (which was external in his prototype). The air chamber certainly brought down the peaky reactive part of the impedance: the result, with chamber, is plotted in Fig. 8.

More familiar to electronics engineers will be the Argand diagram in Fig. 9, where the measured acoustic impedance has been converted into its reciprocal, Z_T, "mobility ohms" as suited to the secondary circuit of Fig. 1b. The value of $R_E/(Bl)^2$ has also been plotted for the CG12, where $R_E=6.5\Omega$ and $Bl=13.7$ T m^{-1}. Maximum power is produced from a constant-voltage generator when Z_T equals $R_E/(Bl)^2$, and energy efficiency is just 50%.

The degree of mismatch between Z_T and $R_E/(Bl)^2$ corresponds to acoustical power loss. If Z_T exceeds $R_E/(Bl)^2$, efficiency does, indeed, rise, but not enough to compensate the drop in load current. If Z_T is less than $R_E/(Bl)^2$, efficiency falls rapidly, with more power being dissipated in the voice coil's ohmic resistance.

The other parameters for the Richard Allen CG12, i.e., moving mass and spring constant, were inserted into the complete electrical network and the equations for acoustical power were solved with the aid of a personal TI-55-II programmable calculator. The resulting frequency response for a 10 V r.m.s. excitation has been plotted in Fig. 10. The maximum predicted output of 5 W may be compared with the 12.3 W that would be developed in an eight-ohm resistance. The 10 V r.m.s. corresponds to a 12 W personal amplifier: the audible effect for bass guitar and concert music is atypical of a domestic 12 W system. The author can credit Klipsch's claim to have achieved a tenfold increase in loudspeaker efficiency over infinite baffle types. For comparison, Fig. 10 also shows the calculated performance of another driver unit (4 ohm), whose Bl factor was much lower at 3.35 T m^{-1}. The lower excitation voltage of 4 V r.m.s. would not develop more than 5 W, but the point to notice is the much more peaky response, showing that the reflected voicecoil resistance has not been located centrally on the Argand diagram in Fig. 9. The klipschorn is capable of handling up to 100 W with less than 1% second-harmonic distortion at 40 Hz (which is mainly due to non-linearity of the air in the throat region (Ref. 5).

The roll-off below 60 Hz looks at first like an admission of failure, but remember that Fig. 10, and Klipsch's own prediction for his Jensen 12A, is based on measurements made on a prototype design. When Klipsch evaluated the final cabinet design, he found that

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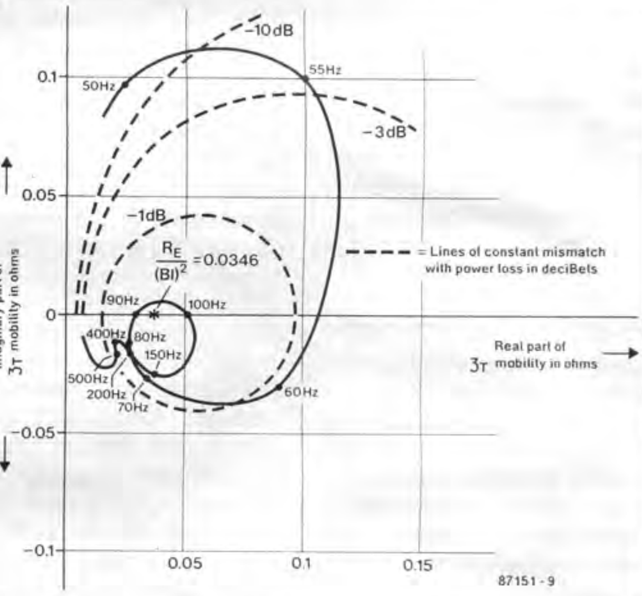

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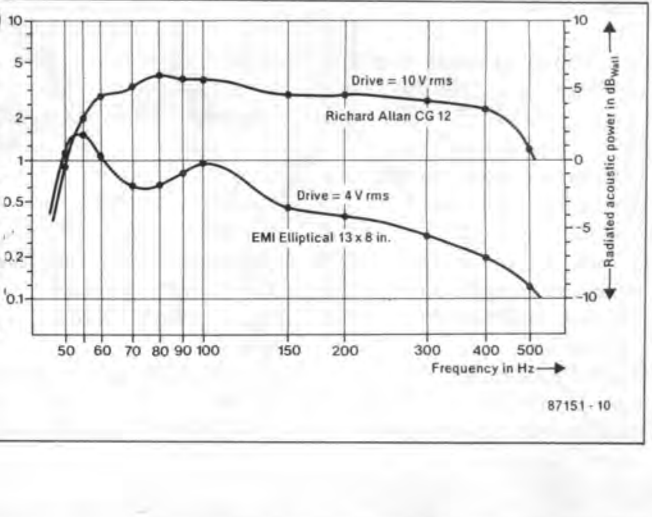

the whole characteristic had shifted fortuitously downwards in frequency, so justifying his claimed "smooth response from 40 Hz to 400 Hz". A crossover is indicated at 400 Hz to a conventional mid-range and tweeter unit: both could be horn-loaded, of course.

Construction

Before tackling this daunting task, the author made two scale models, a 1:8 in cardboard, followed by a 1:3.6 in 3-ply. The working model exhibited a roll-off below 180 Hz, which scaled down to 50 Hz for the full-sized unit. The intrinsically self-bracing structure indicated relatively thin panelling. For cheapness (but not light weight!), half-inch, high-density chip board was used, costing less than £9.00 in all. The truss and some fillets were made in marine 9-ply, while blocking, corner fillets, air seals, and so on were made out of oddments of hardwood and deal.

Joints were glued and screwed except for the access door—one large side panel—which was secured with 14 wood screws. This was necessary for fitting (retrospectively) the CG12 and for possible maintenance. With the door off, the top and bottom fillets would have been precariously unsupported, were it not for centreline fins, which were the author's distinctive (cf. Jecklin, Ref. 6) modification to Klipsch's constructional designs—see Fig. 11, 12, and 13, as well as the accompanying photographs.

References

1. *Paul W. Klipsch, Wireless World*, Feb. 1970
2. Leo L. Beranek, *Acoustics*.
3. Abraham B. Cohen, *Hi-fi Loudspeakers and Enclosures*, 2nd Ed., Newnes Butterworth, London, 1975
4. P.W. Klipsch, *A Low Frequency Horn of Small Dimensions, Journal of the Acoustic Society of America, Vol 13*, pp 137-144 (1941)
5. Rocard 1933 cited in Moire's *Acoustics*
6. *J. Jecklin, Wireless World*, Febr. 1969

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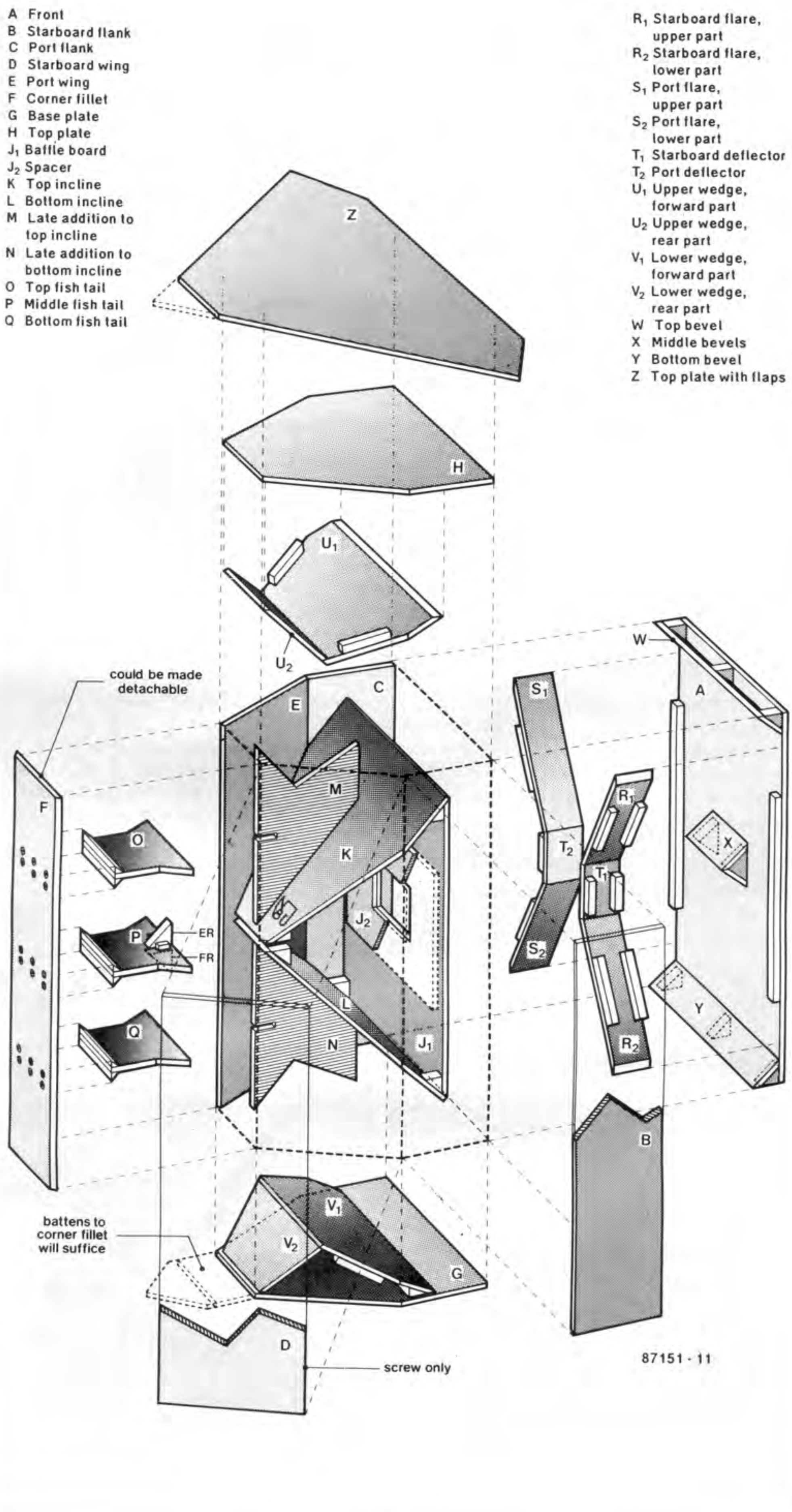

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* C.W. Rice and E.W. Kellogg

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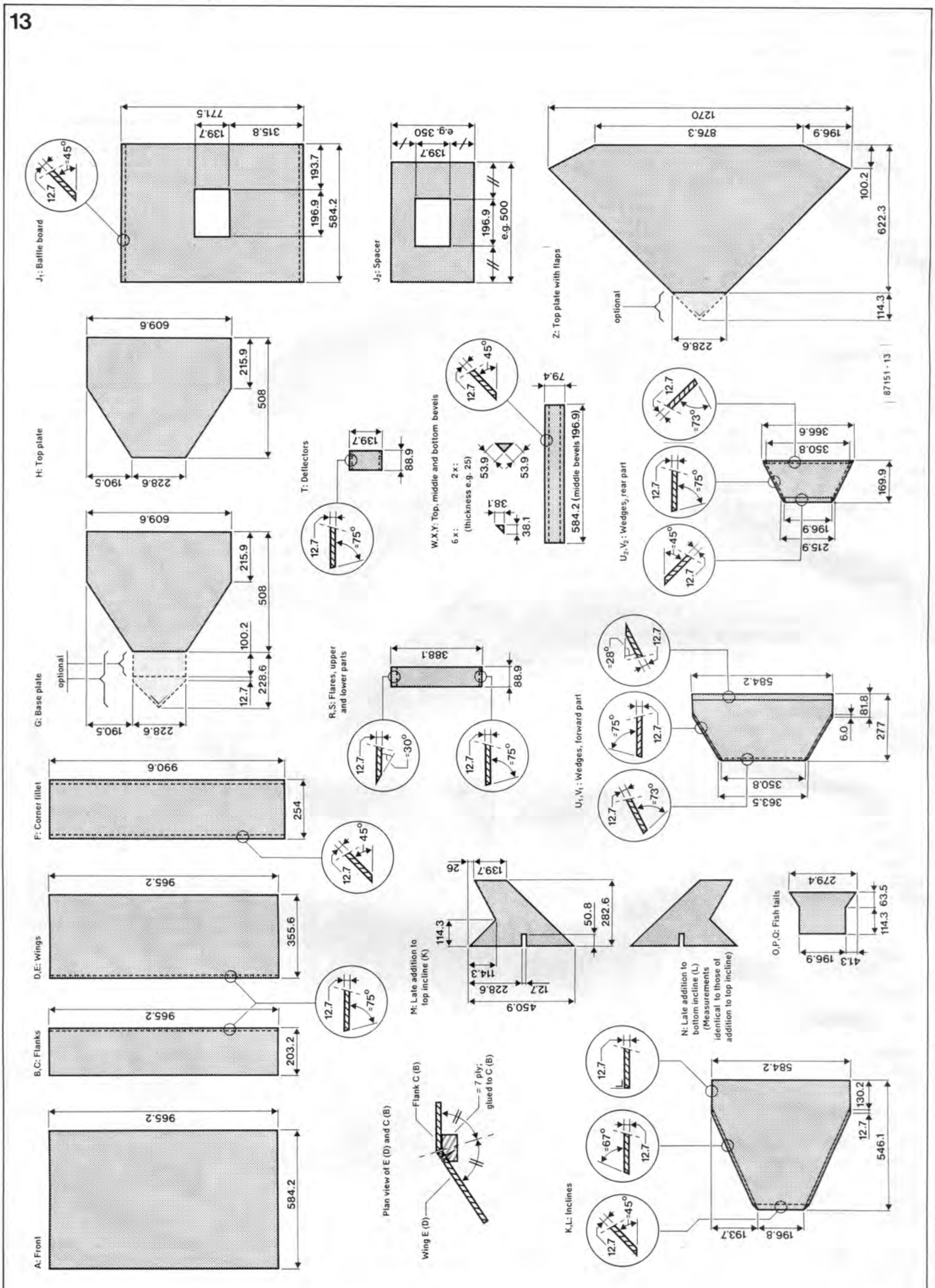

A: Front
965.2
584.2
B,C: Flanks
965.2
203.2
D,E: Wings
965.2
355.6
12.7
≈75°
F: Corner fillet
990.6
254
12.7
45°
G: Base plate
optional
609.6
215.9
508
100.2
12.7
228.6
190.5
228.6
H: Top plate
609.6
215.9
508
190.5
228.6
J1: Baffle board
771.5
139.7
315.8
193.7
196.9
584.2
12.7
≈45°
J2: Spacer
e.g. 350
139.7
196.9
e.g. 500
Z: Top plate with flaps
1270
876.3
196.9
100.2
622.3
114.3
228.6
optional
T: Deflectors
139.7
88.9
12.7
≈75°
W,X,Y: Top, middle and bottom bevels
6 x:
2 x:
(thickness e.g. 25)
38.1
38.1
53.9
53.9
79.4
584.2 (middle bevels 196.9)
12.7
45°
R,S: Flares, upper and lower parts
388.1
88.9
12.7
≈30°
12.7
≈75°
U2,V2: Wedges, rear part
366.6
350.8
169.9
196.9
215.9
12.7
≈73°
12.7
≈75°
≈45°
12.7
U1,V1: Wedges, forward part
584.2
81.8
6.0
277
350.8
363.5
≈28°
12.7
≈75°
12.7
12.7
≈73°
M: Late addition to top incline (K)
139.7
26
114.3
282.6
50.8
114.3
228.6
12.7
450.9
N: Late addition to bottom incline (L) (Measurements identical to those of addition to top incline)
O,P,Q: Fish tails
279.4
63.5
114.3
41.3
196.9
Plan view of E (D) and C (B)
Flank C (B)
≈7 ply; glued to C (B)
Wing E (D)
K,L: Inclines
584.2
130.2
12.7
546.1
193.7
196.8
12.7
≈45°
≈67°
12.7
12.7
87151 - 13

SMA FM STEREO RECEIVER

by F Pipitone

A pocket-size FM stereo receiver built with Surface Mount components.

Surface mount chip Type TDA7021T from Valvo/Mullard is the recently introduced stereo version of the TDA7000 FM receiver decribed in [1]. Together with the TDA7040T stereo decoder, and the TDA7050T AF amplifier—also SMA integrated circuits—the TDA7021T enables building a portable stereo receiver for the FM broadcast band (88 to 108 MHz).

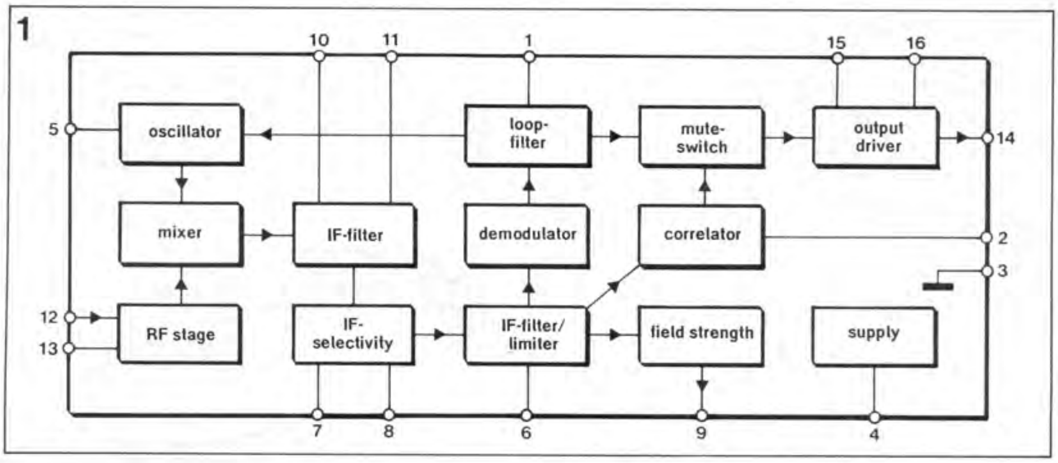


Fig. 1. Internal organization of the Type TDA7021T FM receiver chip.

The internal organization of the TDA7021T is similar to that of the TDA7000, and appears in Fig. 1. The TDA7021T is stereo compatible and has a circuit for indicating the relative signal strength. The chip is housed in a SOT109A enclosure for surface mount assembly. The RF input signal applied to pin 12 is amplified in an RF stage, and subsequently mixed down to the intermediate frequency (IF) with the aid of an externally tuned local oscillator. The IF signal is filtered, given a particular bandwidth, once more filtered, and limited. The limiter drives the field strength indication circuit, whose output controls the mono/stereo switch in the stereo decoder Type TDA7040T. The limited FM signal is also fed to the demodulator and the correlator, which serves to verify correct tuning. The demodulated signal reaches the output amplifier via the loop filter and the mute switch. The local oscillator is tuned externally by a tuned circuit, and internally by the control signal supplied by the loop filter. The principal technical data of the TDA7021T appear in Table 1.

The internal configuration of the stereo decoder Type TDA7040T is shown in Fig. 2. The multiplex signal (MPX) is amplified in opamp A, and cleaned in a 4th order low pass filter with a cut-off frequency of 70 kHz. The pilot tone detector checks whether a stereo signal is being received, and accordingly controls the mono-stereo switch. A phase-locked loop (PLL) is formed by the phase detector, the VCO, and the divider. The latter supplies 4 output frequencies for decoding the stereo signal, and suppressing unwanted signals, such as the VF (Verkehrs Funk) traffic information subcarrier used in Western Germany. The frequency compensation, synchronous demodulator and the matrix ensure that a well-filtered stereo signal is available at the outputs of the chip. The main technical data of the TDA7040T can be found in Table 1.

The third SMA chip in the present FM receiver is the Type TDA7050T stereo AF amplifier—once more consult Table 1.

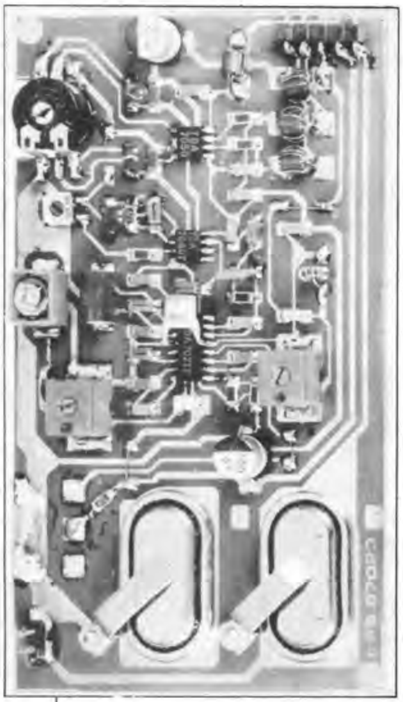
Circuit description

The circuit diagram of the FM stereo receiver is shown in Fig. 3. The RF signal is picked up on the ground return line of the headphone set. Inductors L_4, L_5 and L_6 prevent the RF signal being short-circuited in the supply or the AF amplifiers. The received signal is fed to the RF input on the TDA7021T via C_{14} and parallel tuned circuit C_3-L_1. The local oscillator frequency is determined by the resonance frequency of C_2-C_1-C_{30}-L_2. Trimmer C_1 is the tuning control, while C_2 serves to adjust the tuning range (88-108 MHz). Note that the output of the field strength indicator, pin 9 on IC_1, is connected to the mono/stereo switch input, pin 7 on IC_2. Switch S_1 enables overriding the automatic mono/stereo selector. Preset P_1 serves to set the centre frequency of the VCO in the stereo decoder.

The decoded stereo signal is applied to the AF amplifier via

Technical characteristics.

■ TDA7021T FM receiver.	
Sensitivity (S/N = 46 dB):	300 μV
Channel separation:	53 dB
AF output level:	80 mV
Harmonic distortion (Δf = ±22.5 kHz):	0.7 %
AF bandwidth:	10 kHz
AM rejection:	50 dB
Selectivity S + 300:	30 dB
S - 300:	46 dB
Supply voltage:	1.8 - 6 V
■ TDA7040T stereo decoder.	
Output voltage (U_i = 120 mV):	240 mV
Distortion (stereo):	0.3 %
Channel separation:	40 dB
Signal to noise ratio:	70 dB
19 kHz rejection:	30 dB
38 kHz rejection:	50 dB
57 kHz rejection (SCA):	70 dB
114 kHz rejection (ACI):	90 dB
190 kHz rejection:	85 dB
57 kHz rejection (VF):	75 dB
■ TDA7050T stereo AF amplifier.	
Output power:	75 mW
Distortion (P_o = 10 mW)	1 %
Channel separation:	40 dB
Supply voltage:	1.6 - 6 V



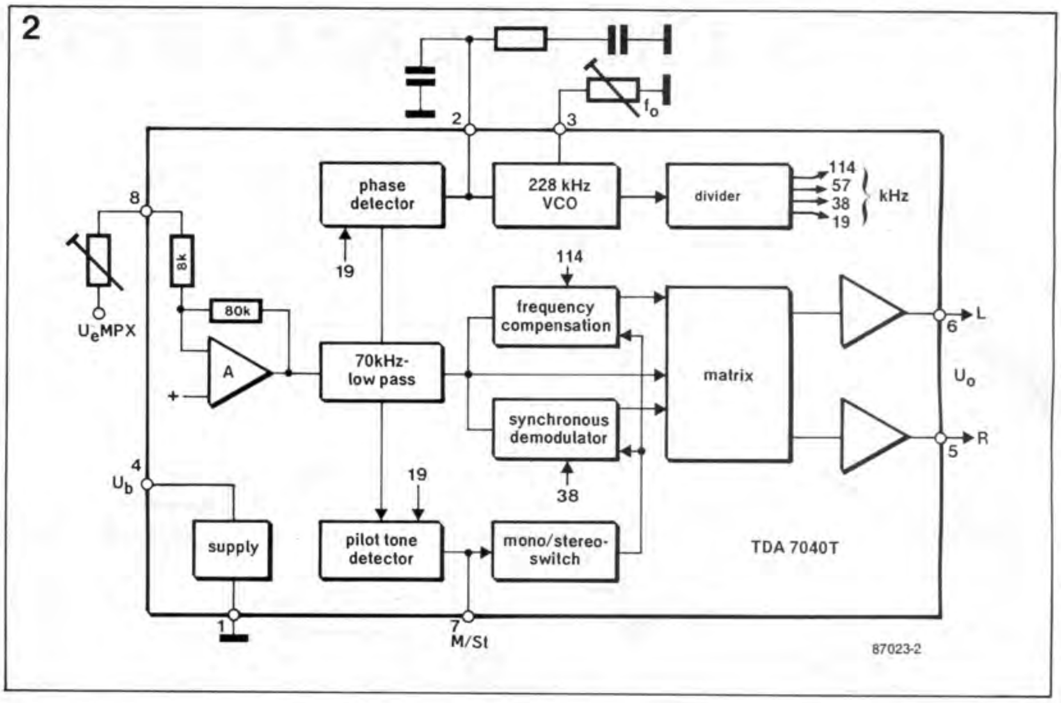


Fig. 2. Internal organization of the Type TDA7040T stereo decoder.

volume controls P_2 and P_3. Resistors R_6 and R_7 at the AF outputs make it possible to connect headphones with a relatively low impedance also.

The receiver is powered by two NiCd button cells which can be charged by the circuit shown in Fig. 4.

Construction and alignment

Great care should be exercised in handling and soldering the tiny SMA components; most of these do not carry a type indication, and are easily lost or mixed up. It is, therefore, recommended not to remove any component from the reel or blister tape, or take it out of its plastic bag, before it is due for fitting onto the PCB. Standard sized components, i.e., non-SMA types, can be used in some circuit positions. This goes for the electrolytic capacitors, tuning capacitor C_1 and the volume controls, P_2 and P_3. Evidently, the application of standard components causes the overall thickness of the receiver to increase.

The ready-made, single-sided, PCB for the SMA stereo receiver is shown in Fig. 5. Use a low-power soldering iron with a small tip to avoid short-circuiting tracks or islands: the free space in between IC terminals is only 0.78 mm!

The SMA components are best fitted with the aid of solder cream, which hardens when exposed to infrared radiation, i.e., heat. The cream is supplied in a syringe to faciliate applying small quantities at a time. A small amount of solder cream is applied onto the track end or soldering island before carefully placing and positioning the relevant component. Even when the cream has hardened, its adhesive force is sufficient to keep the component securely in place. Heat the cream with the soldering iron to make the solder melt, and so ensure a correct joint. Do not apply more heat than is necessary for the solder to creep up the component terminals and flow smoothly across the copper island.

It is also possible to use glue and thin solder instead of

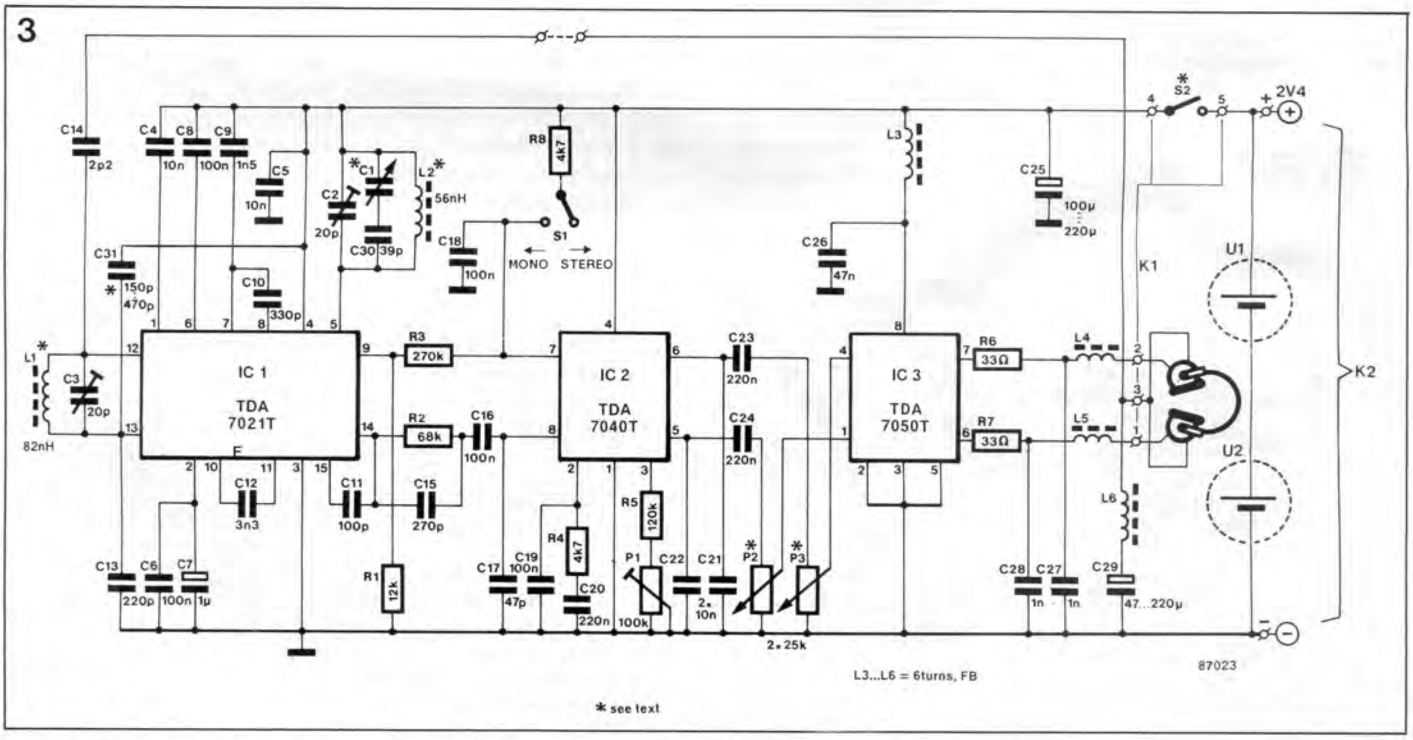


Fig. 3. Circuit diagram of the 3-chip SMA FM stereo receiver.

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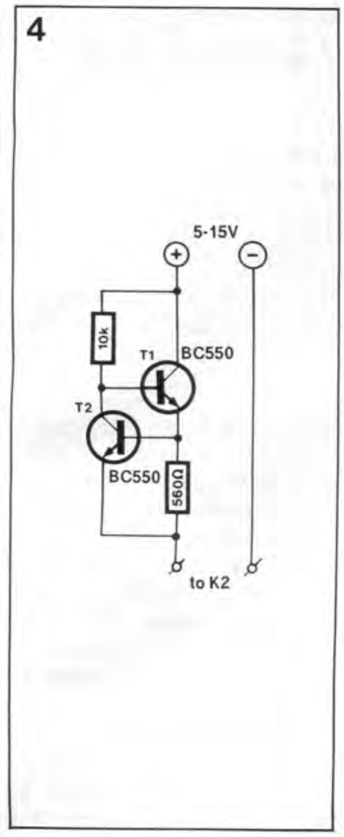

Fig. 4. A simple battery charger.

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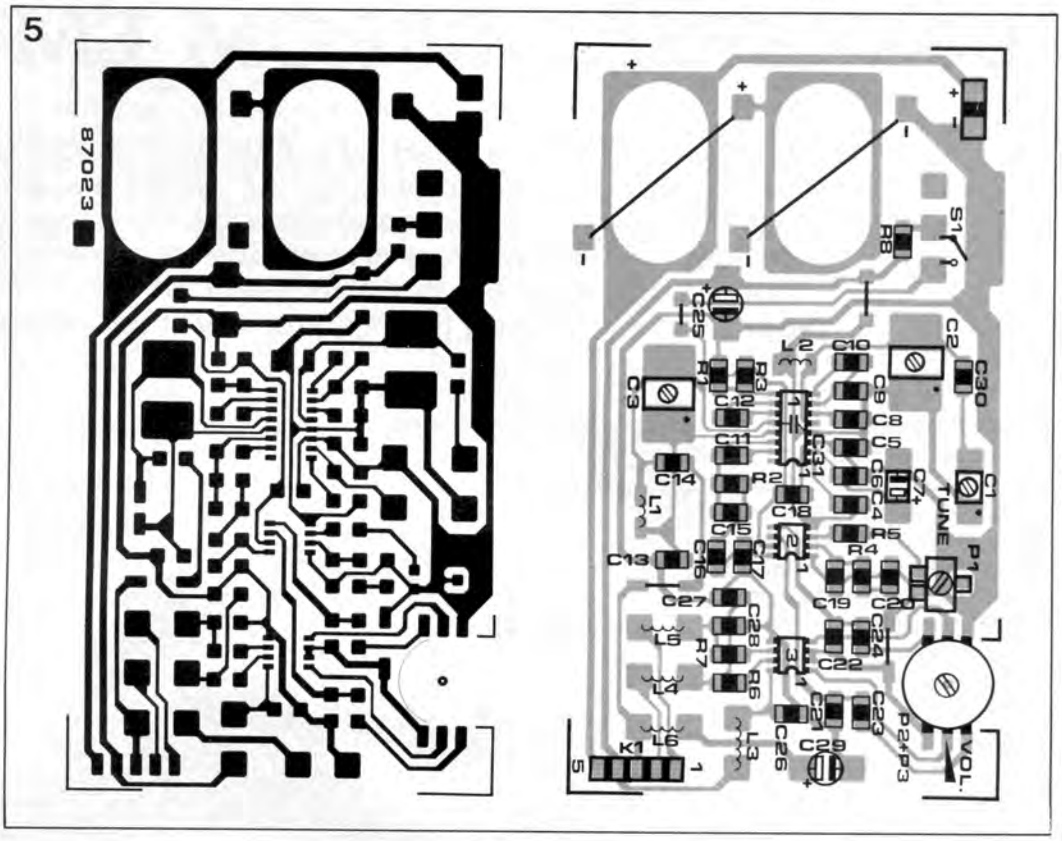


Fig. 5. Track layout and component mounting plan of the PCB for the FM stereo receiver. All parts are fitted at the copper side.

Parts list

Note: all parts Surface Mount Assembly types unless marked ⁺.

Resistors (±5%):
R_1 = 12K
R_2 = 68K
R_3 = 270K
R_4;R_8 = 4K7
R_5 = 120K
R_6;R_7 = 33R
P_1 = 100K preset, e.g. Roederstein type ST 4MB 110k.
P_2^+;P_3^+ = 25K preset ⌀10 mm for horizontal mounting.

Capacitors:
C_1;C_2;C_3 = 20p trimmer, e.g. Stettner Type 30 06 00 584, or Dau Type 445 1k01 025.
C_4;C_5;C_{21};C_{22} = 10n
C_6;C_8;C_{16};C_{18};C_{19} = 100n
C_9 = 1n5
C_{10} = 330p
C_{11} = 100p
C_{12} = 3n3
C_{13} = 220p
C_{14} = 2p2
C_{15} = 270p
C_{17} = 47p
C_{20};C_{23};C_{24} = 220n
C_{25} = 100…220µ; 6 V (value uncritical).
C_{26} = 47n
C_{27};C_{28} = 1n0
C29 = 47…220µ; 6 V (value uncritical).
C_{30} = 39p
C_{31}^+ = 150…470p ceramic (value uncritical).

Inductors⁺:
L_1 = 9 turns 36SWG enamelled copper wire on a T12-12 core.
L_2 = 8 turns 36SWG enamelled copper wire on a T12-12 core.
L_3;L_4;L_5;L_6 = 6 turns 36SWG enamelled copper wire through a 3 mm ferrite bead.

Semiconductors:
IC_1 = TDA7021T
IC_2 = TDA7040T
IC_3 = TDA7050T

Miscellaneous⁺:
S_1 = miniature SPST switch.
S_2 = jumper in headphone plug.
U_1;U_2 = NiCd battery 100 mAh, e.g. Varta Type DK0 100.
Solder cream Multicore flux Sn60 PRMAB3 XCM27298 (Cirkit stock no. 54-22713), or Sn62 PRMAB3 XCM27330 (Cirkit stock no. 54-22712). Both supplied in a 25 g syringe.
Music cassette box.
K_1 = 5-way straight header.
PCB type 87023 (available through the Readers Services).

solder cream, provided it is applied very small quantities, e.g., with the aid of a needle. Do not use instantly dry (super) glue because it does not allow repositioning incorrectly placed components.

Volume controls P_2 and P_3 are standard presets for horizontal mounting, fitted facing one another. A small rectangular piece of metal, plastic or wood is secured in the adjustment slots, and so forms the common shaft of the "stereo" volume control.

If necessary, two SMA capacitors can be fitted next to each other, or one can be fitted on top of the other, to ensure the correct total capacitance. Capacitor C_{31} is a standard ceramic type fitted as close as possible across pins 4 and 13 of IC_1. The wire links are made in thin, insulated or enamelled wire.

It is possible to use a small telescopic aerial instead of the headphone lead for receiving the RF signal: omit the wire link next to C_{13} and connect the aerial output to the soldering island nearest C_{27}.

The receiver may fitted in a modified music cassette box. The headphone connector serves as the on/off switch. Two adjustment wheels with a diameter of 22 mm are cut from a piece of unetched circuit board: one is secured onto the shaft through P_2 and P_3, the other onto the slotted screw on top of tuning capacitor C_1. A part of each wheel protrudes from a slot cut into the side panel of the cassette box.

Trimmer C_2 is adjusted such that C_1 covers the entire FM band (88-108 MHz). Select a weak signal at about 95 MHz, and adjust C_3 for minimum noise. Tune to a relatively strong signal and carefully adjust P_1 for reliable locking of the PLL. The correct adjustment is reached when the noise level increases slightly. *B*

Reference:

(1) *Personal FM*. Elektor Electronics, September 1983.

Note: A number of SMA components for this project is available from Omega Electronics • 252 High Street • Harlesden • London NW10 4TD. Telephone: (01 965) 5748.

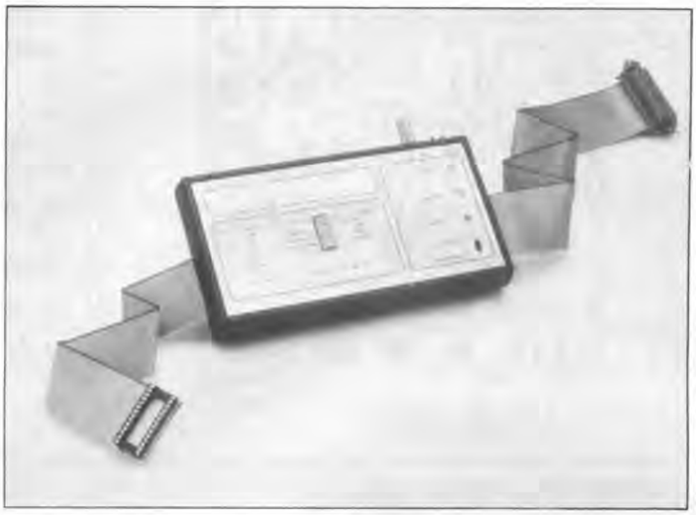
UNIVERSAL EPROM EMULATOR

Any EPROM can be emulated by a RAM with double access: one for reading, and one for writing. The circuit presented here is situated between a host computer and the target system whose resident EPROM software requires fast and efficient editing, that is, without the use of an UV lamp and an EPROM programmer for testing the effect of any small alteration.

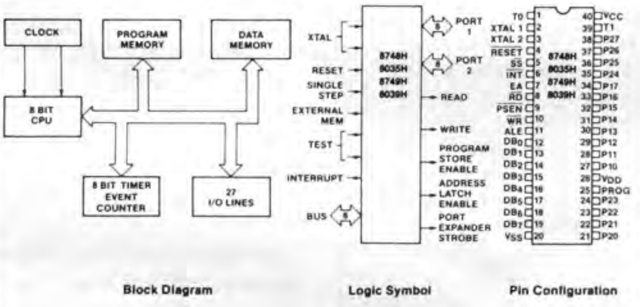
An EPROM emulator can offer a significant time saving to programmers engaged in writing, debugging, or upgrading resident EPROM software. Virtually every computer operator knows that even a single wrong bit in an EPROM may require the device to be taken from its socket, erased with ultra-violet light, verified for complete erase, and entirely re-programmed. Obviously, this is a time consuming procedure that readily ends up in one or more of the EPROM terminals breaking off. The EPROM emulator presented here enables modifying the EPROM contents *while* this is used in the target system. A separate (host) computer is used for editing and filing the contents, and for downloading it into the target system until this runs to satisfaction.

RAM for EPROM

An EPROM emulator is essentially an autonomous block of RAM which can be accessed from two sides simultaneously. For the host system, i.e., the external computer used for editing and downloading the program, this block of memory offers read *and* write access, for the target system read access only. The EPROM emulator therefore comprises a buffered block of RAM whose write enable line can be blocked to simulate the function of a ROM, inserted in the place of the EPROM whose contents require correction or alteration. The EPROM so emulated contains one or more programs or data blocks (look-up tables and the like) that are essential to the operation of the target system. The writing and/or correcting of the EPROM contents is carried out on the host system, which controls and loads the EPROM emulator via a standard serial (RS232) or parallel (Centronics) interface. The target system may be any 8-bit, microprocessor-controlled system, or, indeed, another microcomputer. It is even possible for the host and target system to form part of one and the same computer, which can then modify some of its ROM or EPROM based software via the serial or parallel port. Two EPROM emulators can be operated in parallel to enable working in a 16-bit system. When only one parallel or serial port is available on the computer, the emulators can be connected in turn for alternate editing, filing and downloading of the least significant and most significant databytes.



Device	Internal Memory	
8039H	none	128 x 8 RAM
8035H	none	64 x 8 RAM
8749H	2K x 8 EPROM	128 x 8 RAM
8748H	1K x 8 EPROM	64 x 8 RAM



Block Diagram **Logic Symbol** **Pin Configuration**

87136 - 0

Intel's 8748H/8035H/8749H/8039H microcontrollers

Universal EPROM Emulator

Technical characteristics:

- Emulates EPROM types 2708, 2716, 2732, 2764, 27128 and 27256.
- Direct communication with the target system via a DIP header inserted in the EPROM socket.
- Serial and parallel (RS232 or Centronics) input for downloading EPROM data from the host computer.
- Serial data format: 1 start bit, 8 data bits, 1 or more stop bits. 4 switch selectable baudrates: 1200, 2400, 4800 and 9600.
- Supports 3 file transfer formats with checksum:
  - Intel
  - Tektronix
  - Motorola

  Binary transfer without checksum.
- Visual indication on DATA and READY (transfer complete) line.
- Audible signal for error reports.
- Fast, cost-effective and easy to use.

Access from two sides

The basic operation of the EPROM emulator is shown schematically in Fig. 1. The EPROM whose contents require editing is removed from its socket in the target system, and its place is taken by a header connected to a length of flat ribbon cable carrying the data, address and control lines available in the target system to the EPROM emulator. In this, the address bus is connected to a buffer controlled exclusively by the emulator, while the data bus is connected to a buffer controlled exclusively by the target system. The other side of the buffers is connected to a 32 Kbyte RAM, in which the emulator CPU—a Type 8748H here—places the datawords received from the host computer. To avoid all misconception, it is necessary to keep the functions of host system, EPROM emulator, and target system quite separate. When a complete block of data has been received by the CPU in the emulator, it arranges for the address buffer between the 32 Kbyte RAM and the target system to be enabled, and its own data and address bus to be disconnected from the RAM. Control line $\overline{\text{WE}}$ (write enable) of the RAM is deactivated, while $\overline{\text{CE}}$ (chip enable) is left active. From then on, the relevant area of the 32 Kbyte RAM functions as a read-only memory block in the target system, which gains access to the "EPROM" contents with the aid of lines $\overline{\text{OE}}$ (output enable) and $\overline{\text{CE}}$ via the 28-way flat ribbon cable.

Introducing the 8748H microcontroller.

In view of its specialist nature, Intel's microcontroller Type 8748H has not yet been the subject of an article in *Elektor Electronics*, although it has been on the market for some years already. That shortcoming is rectified in the present article.

The 8748H and Intel's more recently introduced MCS51 series (described in *Single-chip microcontrollers*, elsewhere in this issue) are firmly aimed at electronics specialists, and will form the basis of a number of articles to be featured in forthcoming issues of *Elektor Electronics.*

The 8748H affords good introductory experience with these ready-programmed microcontrollers. It is a less complex and less expensive controller than, say, the 8051, but it is none the less perfectly suitable for a number of small-scale applications, such as the EPROM emulator presented here.

The 8748H is the EPROM version of the mask-programmable 8048, which has found numerous applications in computer keyboards and industrial control systems. Neither the 8748H nor the new MCS51 series can be programmed with an ordinary EPROM programmer, but can only be purchased ready programmed from Elektor Electronics or its agents. These devices, therefore, signal the end of the publication of hexdumps, source listings, and other detailed information on the control program.

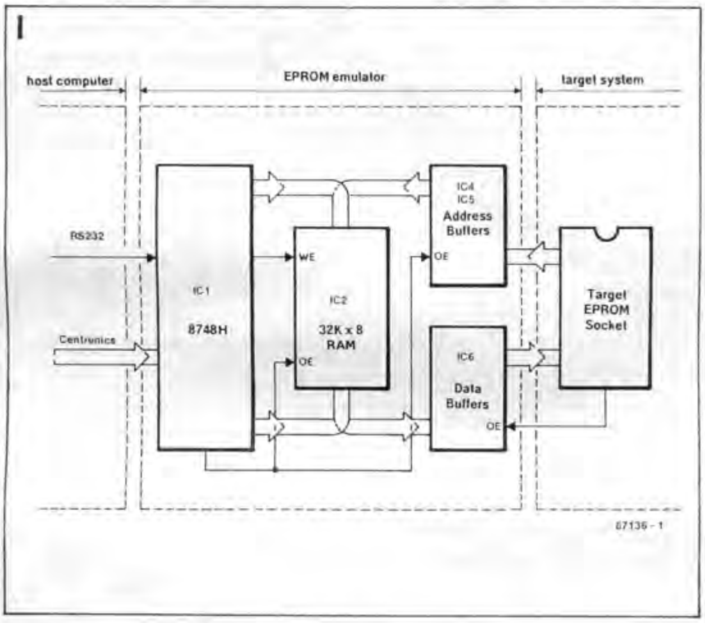


Fig. 1. Illustrating the basic operation of the EPROM emulator.

System control: the 8748H

Briefly recapitulating the foregoing, the EPROM emulator can be considered a quasi-intelligent EPROM which, apart from its data and address bus, has a serial or parallel interface for ready and fast external programming.

The circuit diagram of the programming tool appears in Fig. 2. At the heart of the circuit is the Type 8748H microcontroller, IC$_1$. When the RESET key, S$_{10}$, is pressed, the CPU reads the position of S$_9$ to select between parallel and serial data transfer. The file transfer mode, EPROM type, and serial data speed is read from the configuration of DIL switches S$_1$-S$_8$—see Table 1. The parallel, Centronics compatible, input is complete with 8 data inputs plus the associated strobe line, STRB, and 2 handshaking signals: $\overline{\text{ACK}}$ and BUSY for interfaces activated with the aid of a negative or positive level transition respectively. The non-used outputs PE (paper empty), $\overline{\text{INPUT PRIME RET}}$, and $\overline{\text{FAULT}}$ are forced to the inactive logic level, so that virtually any computer should be able to communicate with the EPROM simulator as if it were a standard printer. It should be noted the K$_1$ is a 36-way header on the PCB for connecting to a Centronics socket on the EPROM emulator. The correct pin connections between these are automatically made with the aid of a length of flat ribbon cable and a 36-way IDC socket. Therefore, the pinning of K$_1$ is **not** identical to that of the Centronics socket.

Since the processor is not fast enough for reading the data on the Centronics input, octal latch IC$_7$ is clocked with the $\overline{\text{STRB}}$ pulse for intermediate data storage, while the bistables in IC$_8$ generate the $\overline{\text{ACK}}$ signal when output P1.7 on the CPU goes high, signalling readiness for reception of a new byte. The presence of a new byte in latch IC$_7$ is signalled to the processor by the negative transition of the inverted BUSY signal, which is applied to input $\overline{\text{INT}}$, and used for lighting LED D$_2$ also, enabling the user to verify reception of data both in the parallel and the serial mode. CPU input T0 is grounded via S$_{9b}$ when the parallel mode is selected. In the serial mode, T$_1$ and D$_1$ convert the RS232 levels on the R×D line into 5 V pulses for driving the INT input on the CPU. It should be noted that the absence of handshaking on the serial input necessitates the use of a number of "zero-modem" wire links on the connector at the host computer side, and this will be reverted to under *Construction*. RS232 handshaking lines are omitted to keep the serial interface simple, without compromising the data transfer speed, which is still fairly high at 9,600 baud maximum.

When an error condition arises, the processor arranges for buzzer BZ$_1$ to be actuated via output P1.1 and MOSFET T$_2$. The READY LED, D$_3$, is illuminated by T$_3$ when the processor activates its P1.2 output. A single RAM chip, IC$_2$, caters for the entire 32 Kbyte memory to enable programming all the EPROMs in the 27XXX series without running into problems regarding the address configurations.

Three buffers are provided for accepting the bus signals from the target system: IC$_5$ and IC$_4$ for the address bus, and IC$_6$ for the data bus. The outputs of these buffers can be switched to the high impedance state by making input $\overline{\text{E1}}$ or $\overline{\text{E2}}$ logic high. The function of IC$_3$ is apparent from the signal applied to pin 11: ALE (address latch enable) is the demultiplexing signal for the databus (D0-D7) and the LS address bus (A0-A7) which share pins 12 to 19 incl. on the 8748H controller.

The target system can only read from the EPROM when IC$_4$ and IC$_5$ are activated by the high level on processor output P1.2. In this condition the RAM can place its data onto the databus, since $\overline{\text{OE}}$ is low together wit $\overline{\text{E2}}$ and $\overline{\text{E1}}$ of the buffers, while demultiplexing latch IC$_3$ is switched to the three-state mode. The target system can activate IC$_6$, and hence read the RAM, by pulling the $\overline{\text{OE}}$ and $\overline{\text{CE}}$ lines on the EPROM socket low.

The rather unconventional central clock frequency of 9.216 MHz (X$_1$) is needed for the timing on the serial input channel, since the 8748H lacks an ACIA based asynchronous communication port. In the present circuit, the processor's interrupt facility is used for reading serial characters. Reception of a serial dataword commences with an interrupt caused by the negative transition of the start bit pulse. When half the start bit period has lapsed, the 8748H starts a counter to introduce a delay corresponding to the period of the start bit. This period depends on the baudrate set with S$_6$-S$_7$. When the delay has lapsed, a new interrupt is generated when the counter counts out. This happens when half the period of the second bit has lapsed. The CPU reads the logic level on the R×D line via T$_1$ and restarts the counter for another bit period, ensuring enough time for processing the received bit, i.e., using it for composing the complete dataword and organizing the hexadecimal file in the memory. This process continues until the last bit of the last dataword has been read into the emulator. The maximum bit rate so achieved is 9,600/s without the use of handshake signals.

2

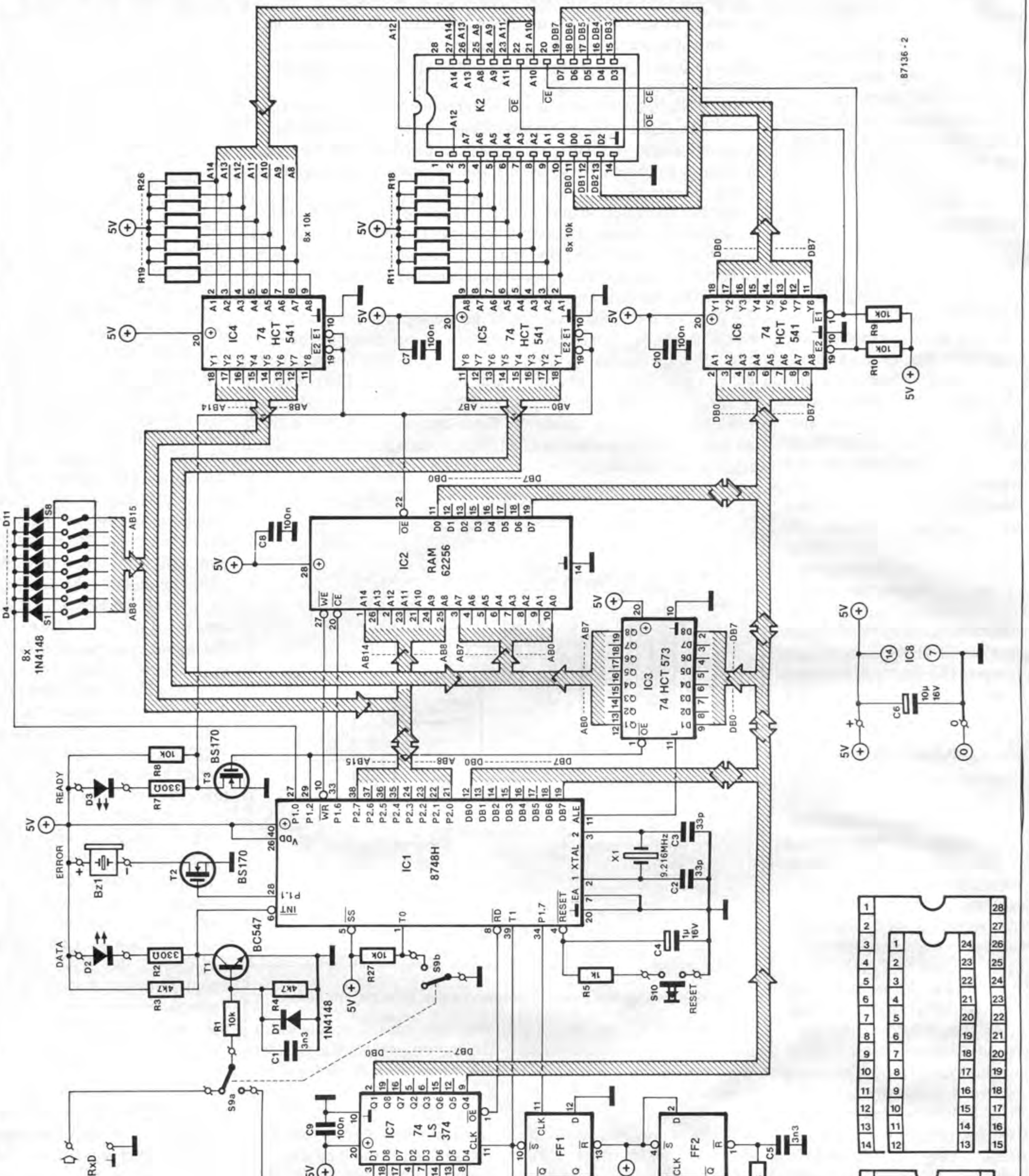


Fig. 2. Circuit diagram of the EPROM emulator.

The CPU clock frequency is determined by the bit period and the internal clock division factors, 15 and 32, of the 8748H. The EPROM emulator draws about 200 mA from an external 5 V supply, which will be part of either the host or the target system in most cases. It is, of course, also possible to build a simple, 7805 based, power supply for the emulator.

3

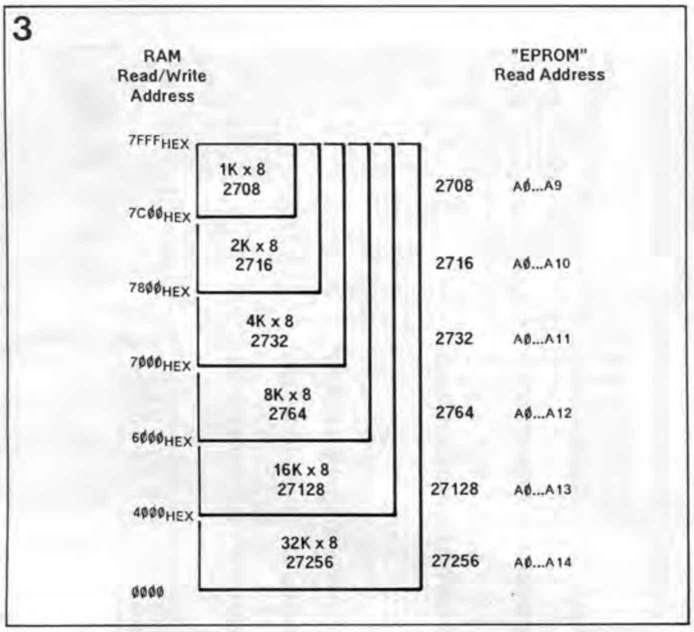


Fig. 3. Memory configurations for the various types of EPROM that can be emulated.

Addressing

Figure 3 shows that substitution of the EPROM in the target system by an external block of RAM requires consideration of the implications of this at the address decoding level. This is briefly discussed in the following four points.

1. If the emulated EPROM has a capacity of less than 32 Kbyte, the corresponding RAM area in the emulator is always located **below** the upper bound of the 32 Kbyte area extending between 0000H and 7FFFH. A Type 2764 8 Kbyte EPROM, for example, is emulated with the aid of memory area 6000H (lowest EPROM address) to 7FFFH (highest EPROM address). Therefore, Fig. 3 distinguishes between the read/write address area of the RAM, and the read-only address areas in the RAM considered EPROM by the target system. All operations in the memory are effected by the 8748H alone, and are invisible to the user.

2. The size of the memory area must always correspond to that of the emulated EPROM. In practice, this means that a 27128, for instance, should not be emulated with the settings of a 2732, or vice versa. The contents of the emulated EPROM are only verified when certain conditions relating to the data transfer are satisfied—this will be reverted to in the section on file formats.

3. Non-used address lines should be left unconnected or made logic high in the target system. When, for example, a 2764 is emulated, the address lines used are A0-A12 incl. (see Fig. 3). The socket pins carrying address lines A13 and A14 should then be made logic high, or left unconnected.

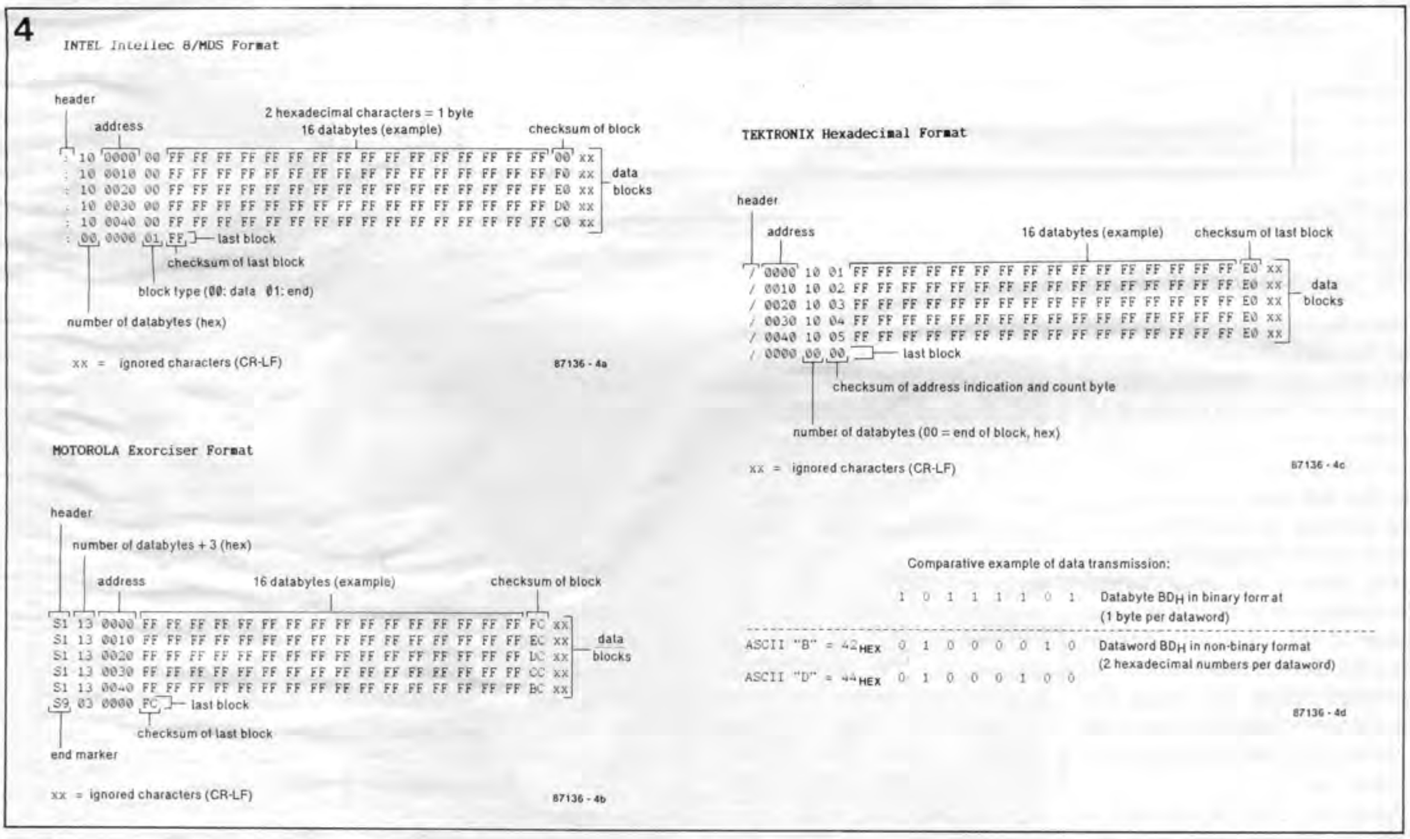
4. In addition to +5 V, the now obsolete Type 2708 needs a +12 V and −5 V supply voltage, both of which may **not** be carried by pins 21 and 19 of the EPROM socket that receives the header from the simulator. When the emulation is finished, the relevant connections should be restored before fitting the (re-programmed) 2708.

File formats

The contents of the emulated EPROM are transferred via the parallel or serial interface. The bit rate on the serial channel, the EPROM type, and the file transfer format are set with DIP switches S_1-S_8 as shown in Fig. 6.

Four file transfer formats are supported by the present EPROM emulator: binary, Intel, Motorola and Tektronix. The least complex of these is the binary format, in which the bytes for the emulated EPROM are transferred sequentially, starting with the lowest and ending with the highest one. The operating system in the EPROM emulator waits for the last byte in the 1, 2, 4, 8, 16 or 32 Kbyte large block of data before the target system can gain access to the RAM. The READY LED is illuminated when reception is complete. The binary transfer format has no verification procedure(s), but is faster than any of the other 3 for-

4


INTEL Intellec 8/MDS Format
header
address
2 hexadecimal characters = 1 byte
16 databytes (example)
checksum of block
data blocks
last block
checksum of last block
block type (ØØ: data Ø1: end)
number of databytes (hex)
xx = ignored characters (CR-LF)
87136 - 4a
MOTOROLA Exorciser Format
header
number of databytes + 3 (hex)
address
16 databytes (example)
checksum of block
data blocks
last block
checksum of last block
end marker
xx = ignored characters (CR-LF)
87136 - 4b
TEKTRONIX Hexadecimal Format
header
address
16 databytes (example)
checksum of last block
data blocks
last block
checksum of address indication and count byte
number of databytes (00 = end of block, hex)
xx = ignored characters (CR-LF)
87136 - 4c
Comparative example of data transmission:
87136 - 4d

```
: 10 0000 00 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF 00 xx
: 10 0010 00 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF F0 xx
: 10 0020 00 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF E0 xx
: 10 0030 00 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF D0 xx
: 10 0040 00 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF C0 xx
: 00 0000 01 FF
```

```
S1 13 0000 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FC xx
S1 13 0010 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF EC xx
S1 13 0020 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF DC xx
S1 13 0030 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF CC xx
S1 13 0040 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF BC xx
S9 03 0000 FC
```

```
/ 0000 10 01 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF E0 xx
/ 0010 10 02 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF E0 xx
/ 0020 10 03 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF E0 xx
/ 0030 10 04 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF E0 xx
/ 0040 10 05 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF E0 xx
/ 0000 00 00
```

```
                  1 0 1 1 1 1 0 1   Databyte BDH in binary format
                                    (1 byte per dataword)
--------------------------------------------------------------------
ASCII "B" = 42HEX 0 1 0 0 0 0 1 0   Dataword BDH in non-binary format
                                    (2 hexadecimal numbers per dataword)
ASCII "D" = 44HEX 0 1 0 0 0 1 0 0
```

Fig. 4. Examples showing the essential characteristics of the various file formats supported by the EPROM emulator. Note that neither the block size of 16 bytes, nor the sequential addressing method of the blocks is imperative.

5

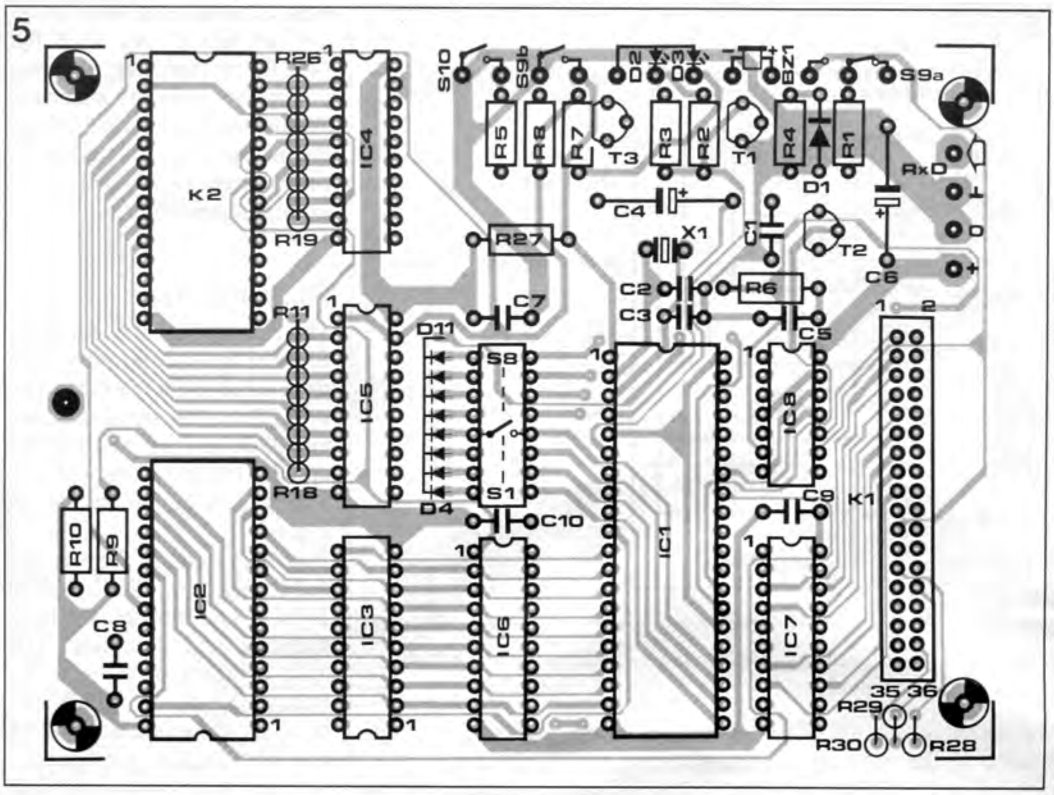
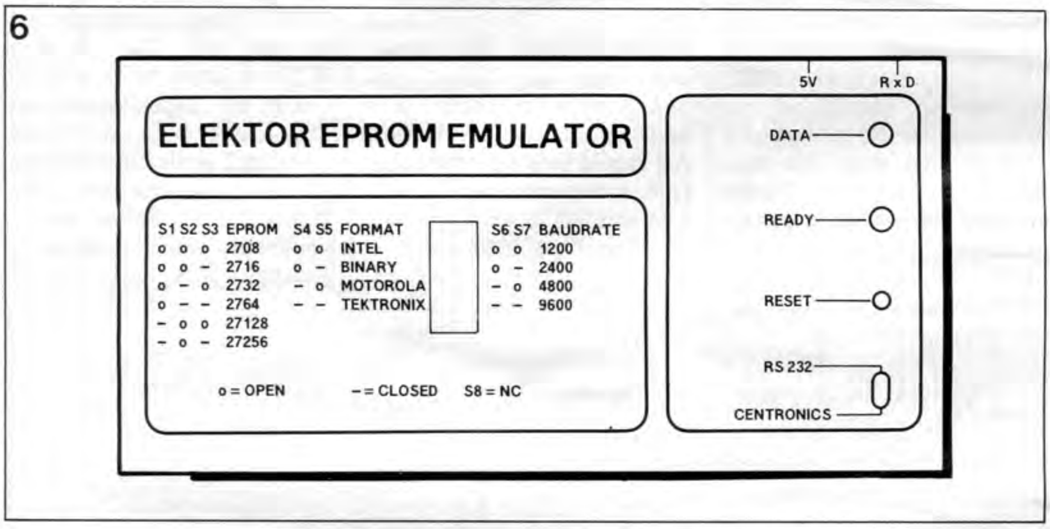


Fig. 5. The printed-circuit board for the emulator.

6



S1	S2	S3	EPROM
o	o	o	2708
o	o	–	2716
o	–	o	2732
o	–	–	2764
–	o	o	27128
–	o	–	27256

S4	S5	FORMAT
o	o	INTEL
o	–	BINARY
–	o	MOTOROLA
–	–	TEKTRONIX

S6	S7	BAUDRATE
o	o	1200
o	–	2400
–	o	4800
–	–	9600

o = OPEN – = CLOSED S8 = NC

Fig. 6. Suggested front panel for the EPROM emulator (foil is NOT available through Readers Services). True width is 178 mm.

mats for updating or loading all or part of the contents of the emulated EPROM. Active buzzer Bz₁ sounds briefly to indicate that the emulator is fed with more data than can be held in the selected EPROM type—no account is taken of the excess bytes. The EPROM emulator should be reset before downloading a new file. Contrary to the standard adopted for the file transfer formats described below, the binary format does not require data to be converted into hexadecimal characters.

When the EPROM emulator is set to operate with the file transfer formats adopted by Intel, Motorola or Tektronix, the target system can only gain access to the emulated EPROM when the 8748H has received and recognized the marker *end of file record*, which, however, need not necessarily signal the end of the EPROM contents. In fact, these formats permit modification of only a number of bytes at EPROM addresses that can be specified by the protocol. This effectively speeds up the downloading process because only parts of the memory to be modified are involved. A further advantage of the above formats is the use of a *checksum*, which enables verifying the reception of correct data. The ERROR buzzer sounds intermittently when a discrepancy is detected. After reception of the *end of file record* marker, the EPROM emulator verifies the contents of the "EPROM", but the buzzer keeps sounding until the RESET key is pressed. Reports of discrepancies between the EPROM data on the host system and those in the emulator's RAM are due either to errors in the transmission, or—less likely—to a checksum error in the original file. In the former case, correct data transfer is readily achieved by once more sending the relevant block to the emulator, while in the latter case an investigation is needed into the operation of the checksummer on the host sys-

Parts list

Resistors (±5%):
R₁;R₈;R₉;R₁₀;R₂₇ = 10K
R₂;R₇ = 330R
R₃;R₄;R₂₈;R₂₉;R₃₀ = 4K7
R₅;R₆ = 1K0
R₁₁ . . . R₁₈ incl.;R₁₉ . . . R₂₆ incl. = 10K SIL networks with 8 commoned resistors.

Capacitors:
C₁;C₅ = 3n3
C₂;C₃ = 33p
C₄ = 1µ; 16 V; axial
C₆ = 10µ; 16 V; axial
C₇ . . . C₁₀ incl. = 100n

Semiconductors:
D₁;D₄ . . . D₁₁ = 1N4148
D₂ = red LED
D₃ = green LED
T₁ = BC547B
T₂;T₃ = BS170*
IC₁ = 8748H (available through the Readers Services).
IC₂ = 62256 or 43256 (32K × 8 CMOS static RAM)
IC₃ = 74HCT573 or 74LS573
IC₄;IC₅;IC₆ = 74HCT541 or 74LS541
IC₇ = 74LS374
IC₈ = 74LS74

Miscellaneous:
X₁ = 9.216 MHz.
S₁ . . . S₈ incl. = DIP switch block.
S₉ = miniature DPDT switch.
S₁₀ = miniature push to make button.
Bz₁ = self-oscillating 5 V buzzer.
K₁ = double-row angled 36-way PCB header.
Mating IDC socket for K₁.
36-way IDC Centronics socket.
K₂ = 28-way IC socket with turned pins.
2 off 28-way DIL headers for press-on (IDC) connection on flat ribbon cable.
PCB Type 87136 (available through the Readers Services).
Suitable ABS enclosure.
Battery-mains socket and plug for external 5 V suppy (e.g. Roca 2.5 mm*).

Note: the front panel foil for this project is not available through the Readers Services.

* Available from Cricklewood Electronics Limited (see p.11)

tem, since the error may well persist no matter how often the block is retransmitted.

Examples of the 3 non-binary file formats are shown in Fig. 4. Each byte is transmitted as 2 hexadecimal numbers, i.e., ASCII characters. Example: dataword BDH is transmitted as 42H followed by 44H, which are ASCII codes for **B** and **D** respectively. Data is organized as *records* consisting of 16 bytes, in accordance with a standardized conversion of each dataword in two hexadecimal characters. When a program for supporting these formats is not available for the host computer used, formatting routines need to be written starting from the guide lines given in Fig. 4. The address transmitted at the beginning of each block is that of the first byte. The header (start character) is not the same for the three formats. In the Intel and Tektronix standards, the count byte gives the number of bytes contained in the block, and is, therefore, 00H in the final block. In the Motorola format, the count byte is the number of bytes in the block plus 3. The checksum in the Intel standard is the 2's complement of the sum of the preceding bytes, including the count byte, address and data. In the Tektronix format, the 2 checksums transmitted for each block are the 8-bit, modulo-256 sum of the preceding 4-bit hexadecimal numbers. Motorola uses yet another verification procedure: here the checksum is the 1's complement of the binary sum of the count byte, address bytes, and databytes. The *end of the block* marker is 01H (instead of 00H) in the Intel mode, and S9H (instead of S1H) in the Motorola convention. Characters received after the checksum of the block, and before the header of the next block, are simply ignored, and can not upset the file transfer.

In the following example it is assumed that the Intel format is used. Each line of 16 databytes results in 43 ASCII characters, followed by the expletive CR/LF sequence, i.e., 45 bytes in all for the transfer. The time needed for transferring a memory area of n bytes at a bit rate B is therefore calculated from

$$(n/16)\times 45\times (10/B) \qquad [\text{s}].$$

Using the Intel format, a file consisting of 4096 bytes can be transmitted in 12 s when the baud rate is 9,600. For the binary format, the time required is simply the EPROM capacity multiplied by $10/n$, i.e., 4 s for 4 Kbytes at 9600 baud.

7

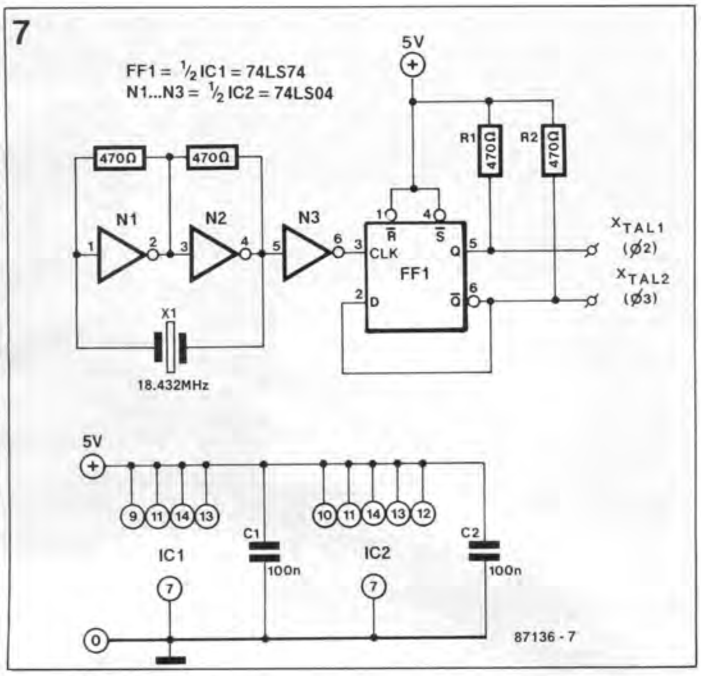


Fig. 7. Build this alternative clock oscillator circuit if a 9.216 MHz crystal is unobtainable.

Table 1.

C	K1	signal	C	K1	signal
1	1	$\overline{\text{DATA STROBE}}$	19	2	GND
2	3	DATA 1	20	4	
3	5	DATA 2	21	6	
4	7	DATA 3	22	8	
5	9	DATA 4	23	10	
6	11	DATA 5	24	12	
7	13	DATA 6	25	14	
8	15	DATA 7	26	16	
9	17	DATA 8	27	18	
10	19	$\overline{\text{ACKNLG}}$	28	20	
11	21	BUSY	29	22	
12	23	PE = "0"	30	24	$\overline{\text{INPUT PRIME RET}}$ = "0"
13	25	"1"	31	26	NC
14	27	NC	32	28	$\overline{\text{FAULT}}$ = "0"
15	29	NC	33	30	NC
16	31	NC	34	32	NC
17	33	NC	35	34	"1"
18	35	NC	36	36	NC

Note: **C** = Centronics connector.
NC = not connected.

8

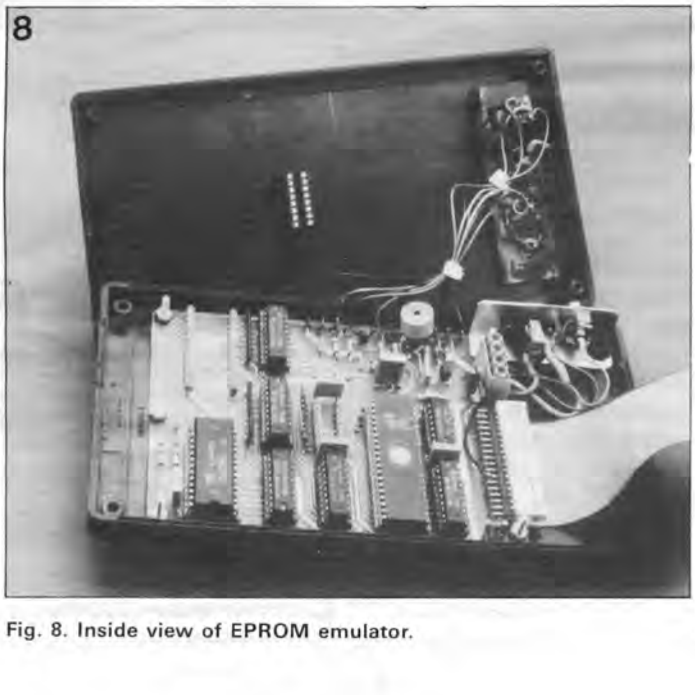


Fig. 8. Inside view of EPROM emulator.

Construction and use in practice

The component mounting plan for the double-sided, through-plated circuit board is shown in Fig. 5. As already mentioned, the pinning of connector K_1 enables ready connection to a Centronics socket via a 36-way IDC header and a length of flat ribbon cable—refer to Table 1. The Centronics or RS232 cable between the simulator and the host computer should not be longer than about 1 metre. The connection between the emulator (K_2) and the EPROM socket in the target system is made with the aid of a 20 to 30 cm long flat ribbon cable terminated at both ends in a high quality 28-way DIP header. It is possible to omit K_2 and solder the header straight into the relevant holes in the PCB. It is advisable to check the correct connections between the systems, and to mark pin 1 of the target header in write paint to avoid all confusion.

All parts are soldered onto the PCB, except the 2 LEDs, S_9, S_{10} and the self oscillating buzzer. Diodes $D_4 \ldots D_{11}$ incl. are fitted vertically with the cathodes pointing upwards and commoned by a length of horizontally running wire. The same mounting method applies to R_{28}, R_{29} and R_{30}, and also for $R_{19} \ldots R_{26}$ incl. and $R_{11} \ldots R_{18}$ incl. if suitable SIL type resistor networks are not available. IC_7 and IC_8 should be low power Schottky (LS) types in view of the possibility of their inputs remaining unconnected. These 2 ICs can be omitted if it is not intended to use the parallel input of the EPROM simulator. All other integrated circuits can be LS or HCT types. Make sure that IC_3 and RAM IC_2 are fitted with the correct orientation on the PCB. The power supply connection to the board is made either direct in relatively strong wire, or via a 2-way edge connector with screw terminals. As to the enclosure that houses the EPROM emulator, the photographs in this article should give some idea of the practical realization. Whatever housing is used, make sure that the DATA and ERROR LED are mounted such that their visibility is ensured from relatively far, and also that S_{10} is within easy reach. It is recommended to have the DIP switches protrude from the top panel to enable rapid changes of the settings. Figure 6 shows a possible layout for the pront panel of the emulator.

It was already noted that the 9.216 MHz crystal may be a difficult-to-find component. Fig. 7 shows a suggestion for an alternative clock oscillator based on a 18.432 MHz crystal. It should be noted that this circuit can not be located on the PCB for this project, and therefore needs to be built separately on a piece of Veroboard. It is important to have both the emulator and the target system powered when the connection between them is installed or removed.

As already suggested, a zero-modem configuration is used for the handshaking sigals on the RS232 interface if this is used for loading data into the EPROM emulator. Output signal RTS (*request to send*, pin 4) is connected direct to input CTS (*clear to send*, pin 5), and the same goes for DTR (*data terminal ready*, pin 20) and DCD (*data carrier detect*, pin 8). If necessary, DSR (*data set ready*, pin 6) is connected to DTR-DCD. These connections should enable the RS232 interface to function as if there were real handshaking signals.

Whatever computer or computer-based system is emulated with the present EPROM emulator, both units should be powered before being interconnected. Initialize the EPROM emulator by pressing the RESET key before transferring a new data block or file. The initialization has no effect on the RAM contents, but informs the 8748H that a new block of data is imminent. Also do not forget to press RESET after making any change in the DIP switch settings.

A 8748 based serial EPROM programmer will be described in a forthcoming issue of *Elektor Electronics*.

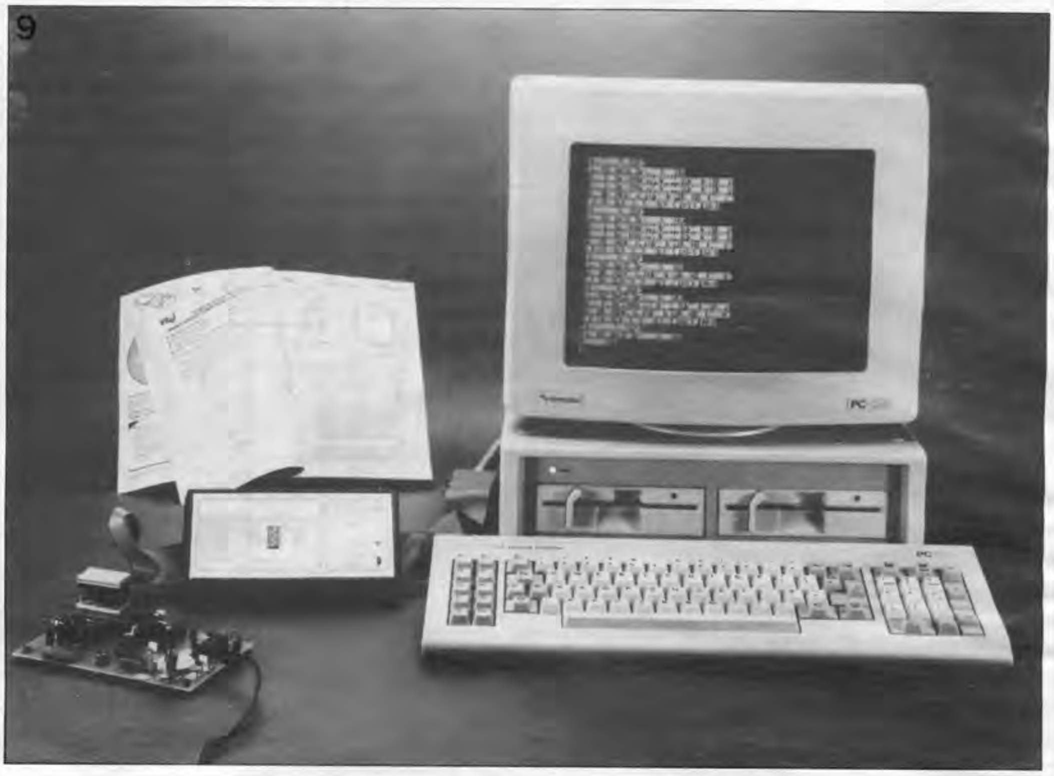


Fig. 9. A prototype of the EPROM emulator used in conjunction with an Amstrad PC1512 host computer.

EW PRODUCTS • NEW PRODUCTS • NEW

Function generator is fully GPIB programmable

New from Electronic Brokers is the Thandar Model TG401, a 4 MHz function generator which is fully GPIB programmable.

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The instrument is IEEE-488 compatible and codes and formats are according to IEEE-728. It operates as a listener and talker with extended subset capabilities.

Use of extended software enables very clear operation. An easy to understand panel design minimises possible operating errors. If a frequency or amplitude/offset is programmed, the generator will automatically set it to the optimal range. If data entered is not at full possible resolution, the TG401 will allocate a full display resolution. A corresponding error message indicates incorrect settings or syntax errors.

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ACTIVE PHASE-LINEAR CROSS-OVER NETWORK

The ideal cross-over network is free of phase-shift, resulting in optimum pulse performance and radiation pattern. Although the ideal is not yet within reach, the work of Stanley Lipshitz and John Vanderkooy enables it to be approached very closely.

The most serious problem with ordinary cross-over filters is best illustrated with reference to a two-way system. This consists of a low-pass and a high-pass filter. One of the properties of a low-pass section is that it causes a time-delay of the signal. A high-pass filter on the other hand causes an acceleration of the signal. These actions result in a number of complications at the cross-over point:

(a) the signals from the two sections partially cancel one another;
(b) the strongly varying phase shift between the two signals adversely affects the radiation efficiency of the overall system;
(c) the radiation pattern becomes frequency dependent.

Some years ago, Stanley Lipshitz and John Vanderkooy published a series of papers ([1, 2, 3]) that have laid the foundation of the so-called phase-linear cross-over network.

Basically, the phase-linear network uses a low-pass section that also provides a high-pass characteristic with the aid of a time-delay and subtraction circuit. True, the time-delay is not constant over the entire frequency range, but it varies only slowly; moreover, there are no phase differences between the two output signals, even near the cross-over frequency.

A block schematic of a two-way, as well as a three-way, system based on the work of Lipshitz and Vanderkooy is shown in Fig. 1. It should be emphasized that the time-delay is an essential facet of the design. There are filters that make use of the subtraction method only, but these do not exhibit phase linearity.

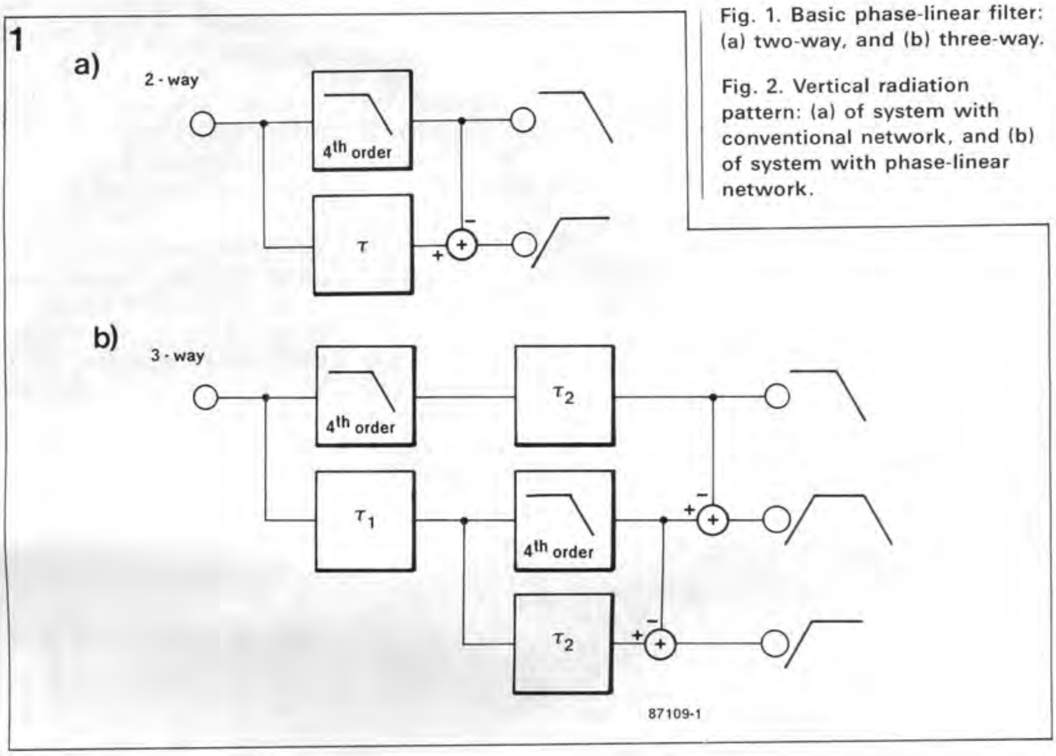
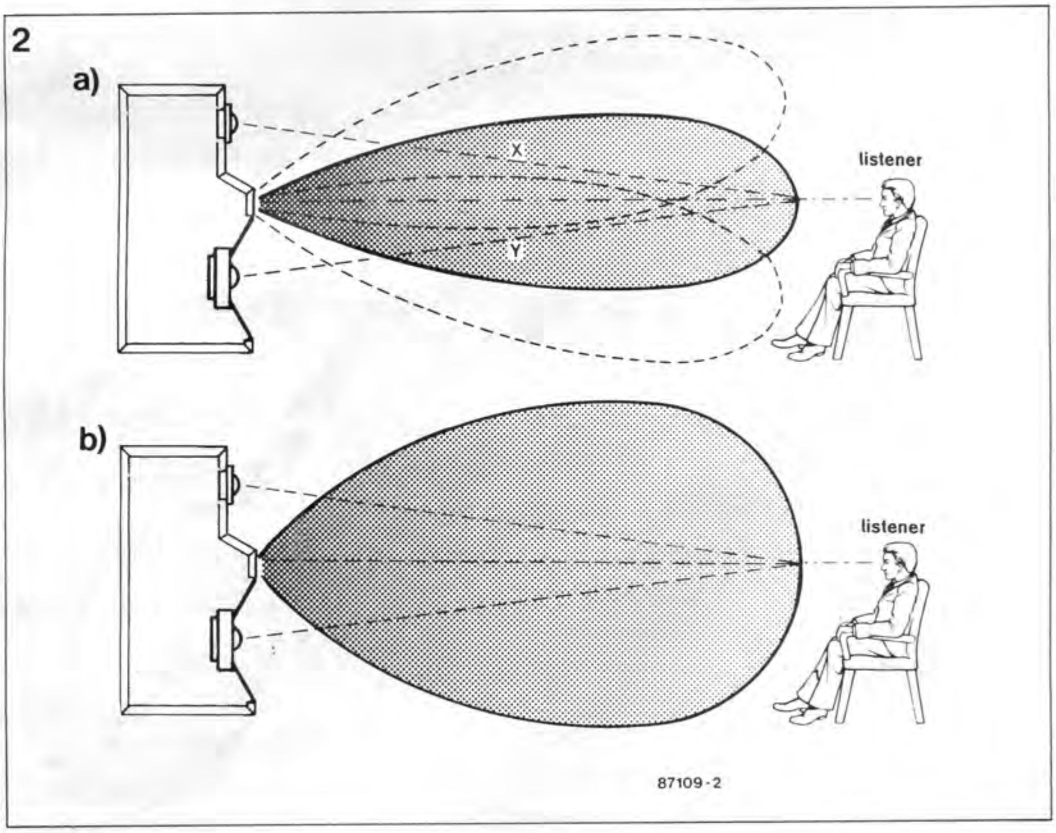


Fig. 1. Basic phase-linear filter: (a) two-way, and (b) three-way.

Fig. 2. Vertical radiation pattern: (a) of system with conventional network, and (b) of system with phase-linear network.



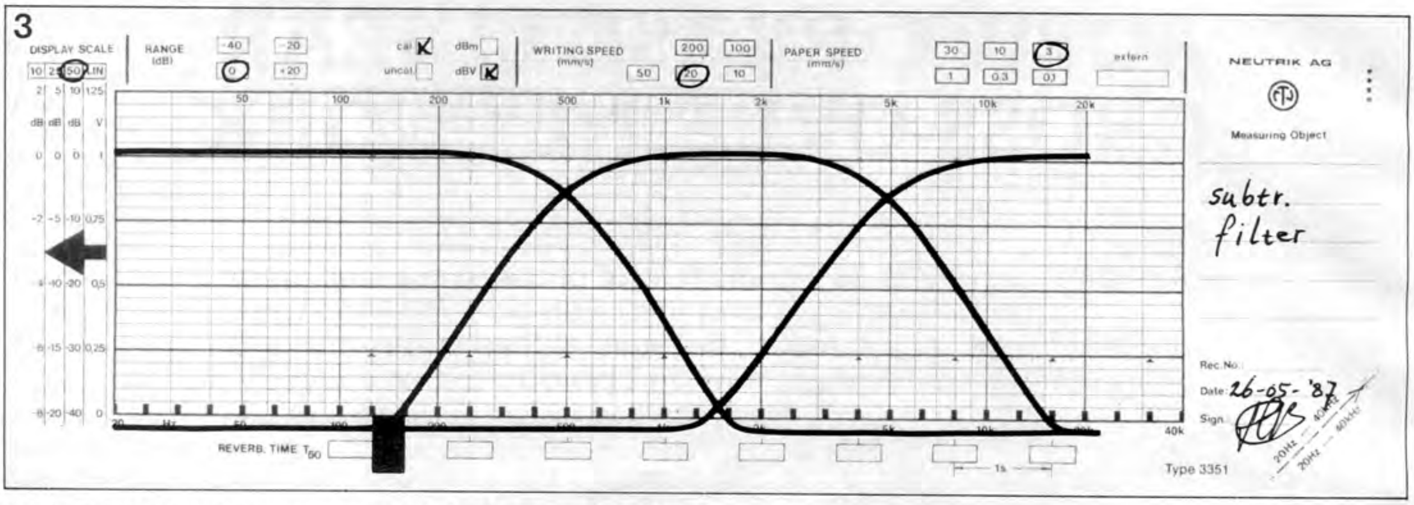


Fig. 3. Amplitude vs frequency characteristic of a three-way phase-linear network.

A customary fourth-order low-pass filter in the upper branch provides the normal low-pass performance. The delay, τ, is designed such that it has exactly the same phase behaviour as the low-pass section, and functions as an all-pass section. When then the output signal of the low-pass section is subtracted from the delayed signal, the result is a high-pass characteristic that has the same phase behaviour as that of the low-pass filter. Summing the two signals results in a perfectly straight line.

The set-up of a three-way system—see Fig. 1b—is a little more complicated, because an additional low-pass section has to be provided in the centre limb to obtain a band-pass characteristic for the middle frequency loudspeaker. This additional section must be compensated by a second delay, τ_2. Thus, in a three-way system, the τ_1 circuit simulates the time delay of the usual bass filter, while the τ_2 delay simulates the delay of the low-pass filter in the middle-frequency section.

The vertical radiation pattern (polar response) of a conventional loudspeaker system is shown in Fig. 2a. The dispersion is fairly small in the region where both speakers provide a signal. The spread also varies with frequency, which causes the lobe to either tilt or sag. The pattern of the phase-linear system in Fig. 2b shows that the lobe is much broader and points forward at all frequencies. In all this it is assumed that the acoustic centres of the loudspeakers lie on a vertical line, otherwise the pattern deteriorates.

A practical network

In a practical network, it is not possible (at least with an ac-

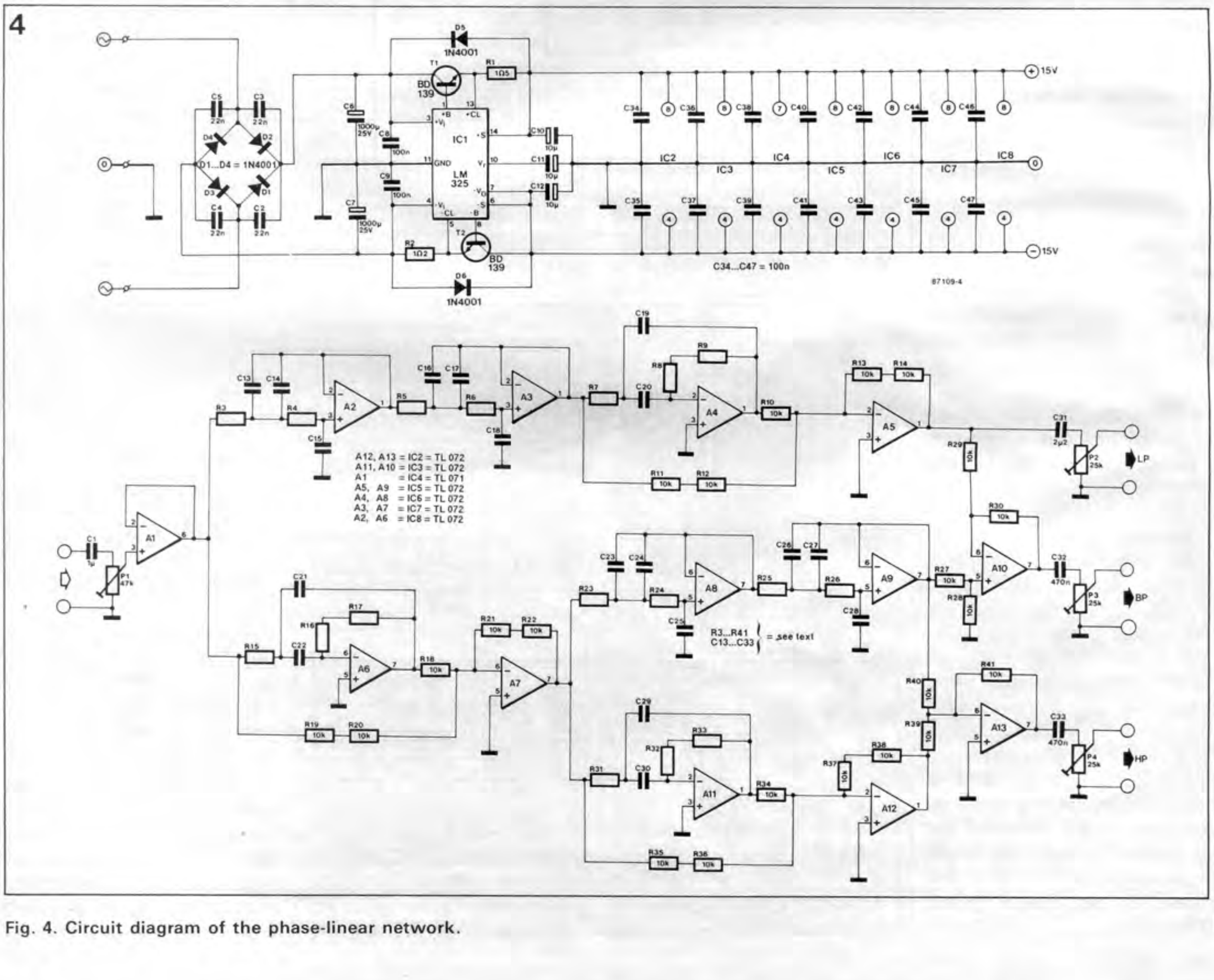


Fig. 4. Circuit diagram of the phase-linear network.

5

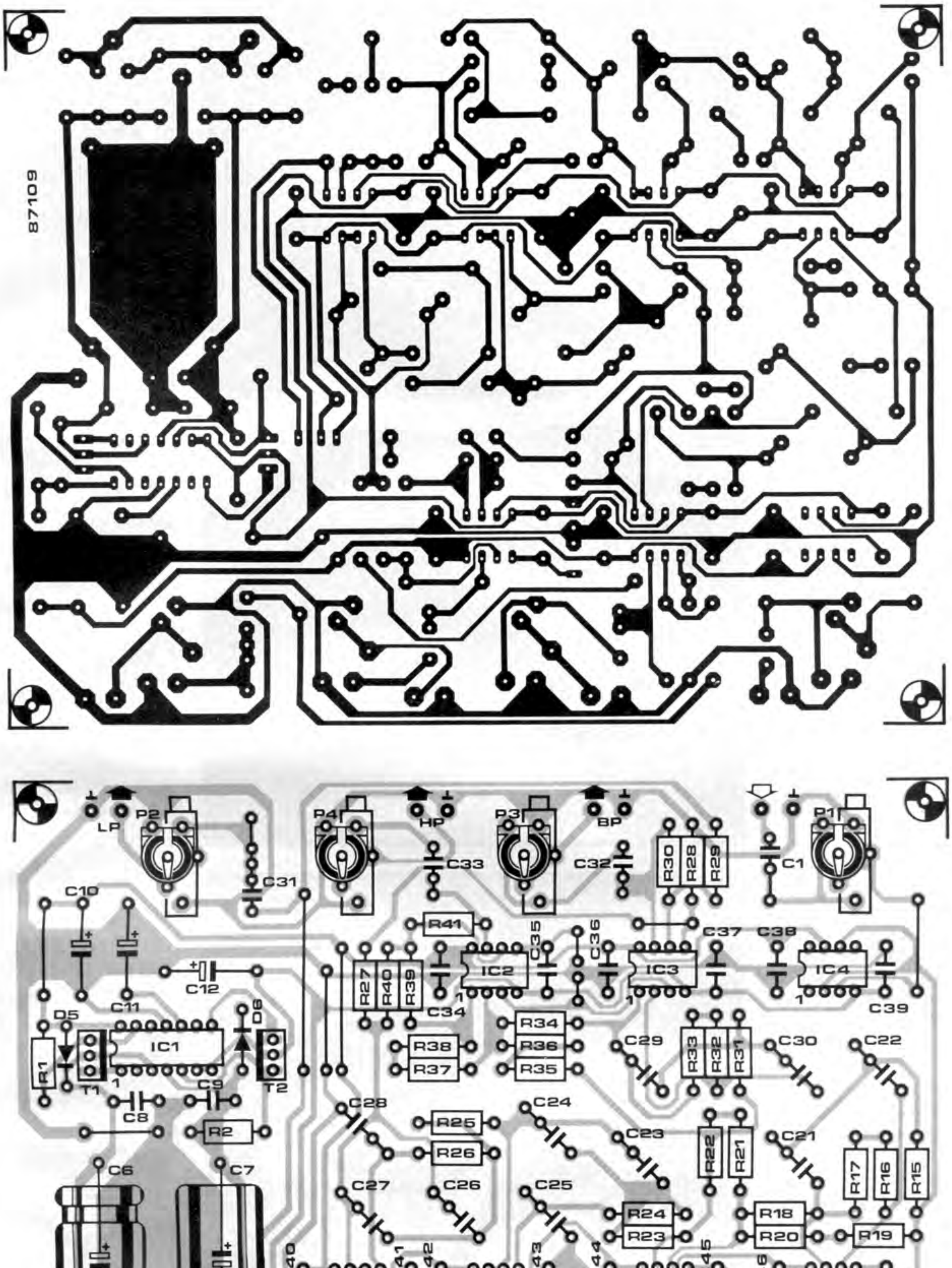


Fig. 5. Printed circuit board of the phase-linear filter.

ceptable number of components) to simulate any phase behaviour with the aid of a delay circuit.

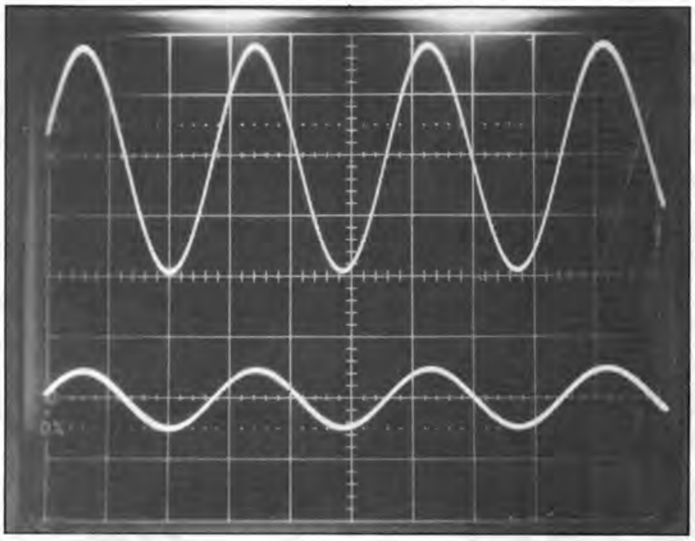
All-pass networks have some interesting properties:

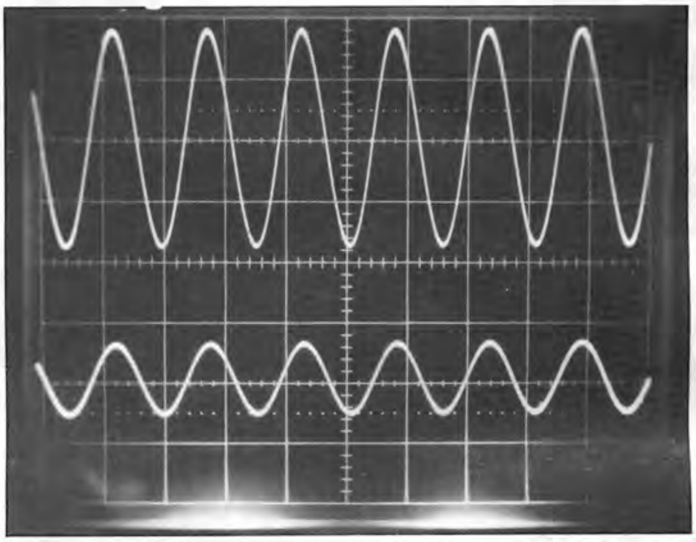
(a) they cause a phase shift, but no signal attenuation over a given frequency range;
(b) the phase shift caused by them is twice as large as that caused by a filter of the same order.

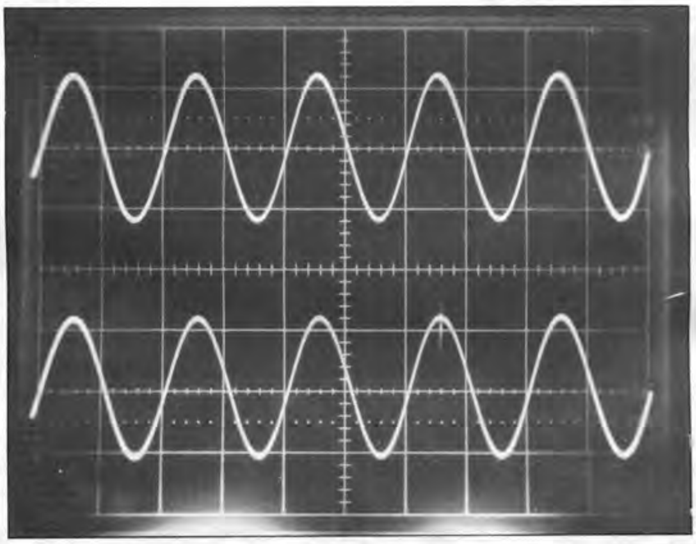
From this, it is evident that the low-pass section should be an even-order type, i.e., second-, fourth- or sixth-order. In the present network fourth-order filters are used, since these give a sufficiently steep roll-off and do not unnecessarily complicate the circuit.

Like all fourth-order networks, the present consists of a cascade of two second-order filters. For the present purposes, these should be identical to ensure that the phase behaviour of the all-pass network will be the same as that of the filter.

It was found that the Linkwitz-Riley (Squared Butterworth) filter is eminently suitable for the present network, because it allows a fairly simple all-pass to be designed with only two opamps. The resulting circuit has exactly the same phase behaviour as a fourth-order Linkwitz low-pass filter. Note that the cross-over frequencies are −6 dB points (as in all Linkwitz filters), since there is no phase shift between the two channels. The relative amplitude vs frequency characteristic is given in Fig. 3, while the three photographs illustrate the typical performance of the network. The photographs show the output voltage at the low- and middle-frequency terminals (a) slightly below the cross-over point, (b) at the cross-over point, and (c) slightly above the cross-over point. No phase differences between the two signals are discernible anywhere.







Circuit description

In the circuit diagram of Fig. 4, opamp A_1 is used as a buffer between the input signal and the filter proper. If necessary, the input signal may be attenuated by P_1; the total amplification of the network is unity.

The low-pass filter is constructed around A_2 and A_3, while the associated all-pass filter is based on A_6 and A_7. The attenuation due to band-pass filter A_6 is compensated by A_7. The low-pass section for the middle frequencies consists of A_8 and A_9. Here, two identical all-pass filters are required, and these are formed by A_4-A_5 in the low section and by A_{11}-A_{12} in the high section. That completes the low-pass filter.

For the middle-frequency section, the output signal of A_5 must be subtracted from that of A_9, which is effected by A_{10}. Finally, the output signal of A_9 is subtracted once more from that of A_{12}, which is done by A_{13}. That completes the high-pass function.

The three outputs of the network are taken to preset potentiometers that enable matching each of them to the efficiency of the associated loudspeaker.

The quality of the power supply matches that of the cross-over network itself. Circuit IC_1 is a voltage regulator, which, in conjunction with two external series transistors, provides symmetrical output voltages. Diodes D_5 and D_6 ensure that the regulator is not damaged at switch-off.

Parts list

Resistors:

R_1;R_2 = 1K5J
R_3 to R_9; R_{15} to R_{17}; R_{23} to R_{26}; R_{31} to R_{33} = 22K5F
R_{10} to R_{14}; R_{18} to R_{22}; R_{27} to R_{30}; R_{34} to R_{41} = 10KF
P_1 = 47KJ cermet preset
P_2 to P_4 = 25KJ cermet preset

Capacitors:

C_1 = 1μ0 plastic film
C_2 to C_5 = 22n ceramic
C_6;C_7 = 1000μ; 25 V electrolytic
C_8;C_9;C_{34} to C_{47} = 100n ceramic
C_{10} to C_{12} = 10μ; 25 V electrolytic
C_{13} to C_{18};C_{21};C_{22} = 10n; 2.5% polypropylene
C_{19};C_{20};C_{23} to C_{30} = 1n0; 2.5% polypropylene
C_{31} = 2μ2 plastic film
C_{32};C_{33} = 470n plastic film

Miscellaneous:

PCB Type 87109 (readers who wish to make their own PCB may order the relevant drawings free of charge on the Order Form on page 69).

NOTE: Many components may be available from
Audiokits Precision Components
6 Mill Close
Borrowash
DERBY DE7 3GU
Telephone: (0332) 674929

Semiconductors:

D_1 to D_6 = 1N4001
T_1 = BD139
T_2 = BD140
IC_1 = LM325
IC_2;IC_3;IC_5 to IC_8 = TL072; NE5532; LF353; LM833, OP215
IC_4 = TL071; NE5534; LF356; OP27; OP15

Construction

The network is most conveniently constructed on the ready-made PCB Type 87109 shown in Fig. 5. The values of the components given in the parts list pertain to cross-over frequencies of 500 Hz and 5,000 Hz. Different frequencies may be calculated with the aid of the Linkwitz formulas in Ref. 4.

In several places, capacitors are shown in parallel and resistors in series: this is done to enable the use of as many components of the same value as possible. As usual, the choice of capacitors is determined mainly by their loss factor and cost, which normally results in plastic film types.

It should be noted that each PCB has its own regulator IC: this is convenient where the network is fitted in the loudspeaker enclosure.

The impedance at the network outputs, depending on the position of the presets, has a maximum value of 12 kilohm. Since this may be on the high side for certain output stages, the value of the presets may be reduced to 5 kilohm, which results in a maximum output impedance of 2.5 kilohm. Where this is done, the value of C_{31} should be increased to 4µ7. A useful rule of thumb is that the input impedance of the output stage must be at least ten times as large as the output impedance of the network.

The PCB may be used to construct a two-way network, in which case the following components are omitted: IC_2; IC_5; IC_6; R_7 to R_{14}; R_{23} to R_{26}; R_{31} to R_{41}; C_{19}; C_{20}; C_{23} to C_{30}; C_{33}; P_4. Furthermore, a wire link should be fitted between pin 1 of A_3 and another between pin 7 of A_7 and C_{32}.

References

1. S. Lipshitz & J. Vanderkooy, *A Family of Linear-Phase Cross-over Networks of High Slope Derived by Time Delay* (*Journal of the Audio Engineering Society*, Jan. & Feb. 1983).

2. S. Lipshitz and J. Vanderkooy, *Is Phase Linearization of Loudspeaker Cross-over Networks Possible by Time Off-set and Equalization?* (*JAES*, Dec. 1984)

3. S. Lipshitz and J. Vanderkooy, *Use of Frequency Overlap and Equalization to Produce High-slope Linear-phase Loudspeaker Cross-over Networks*, (*JAES*, March 1985)

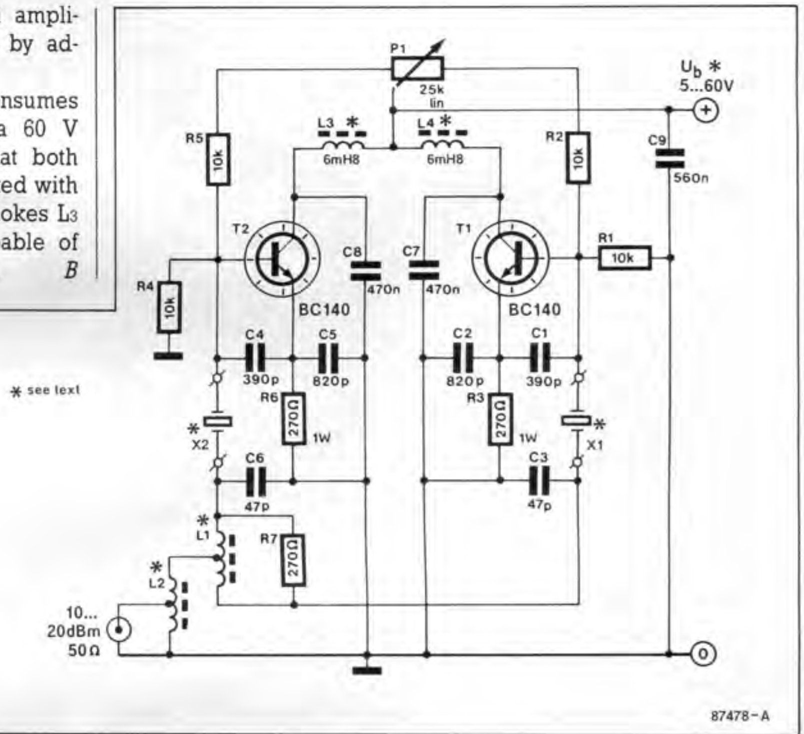
4. *Linkwitz Filters, Elektor Electronics*, April 1987

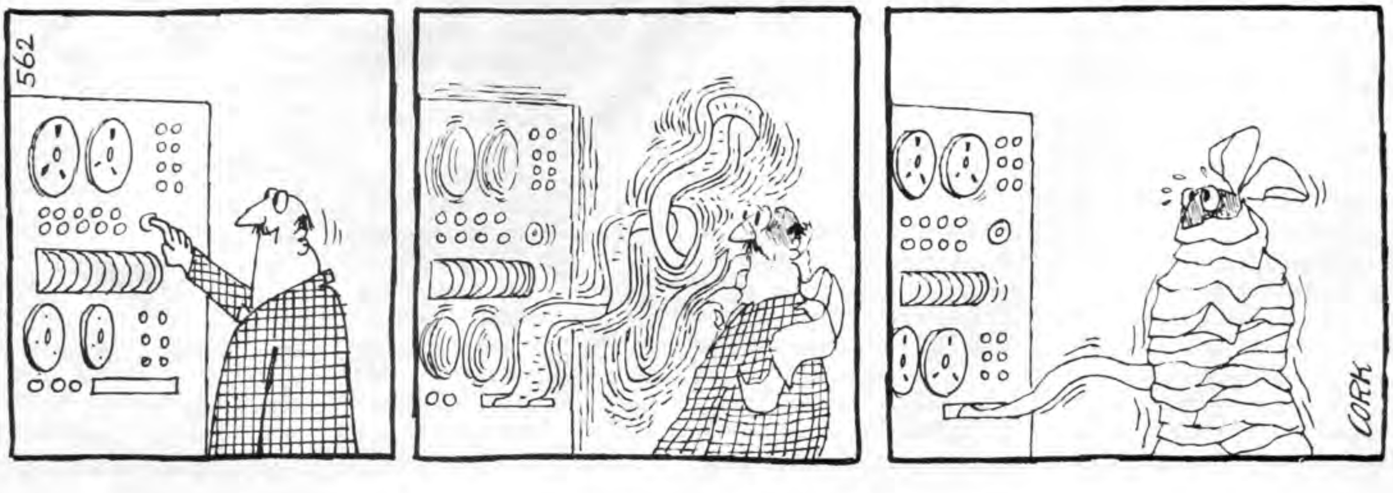
90

TWO-TONE RF TEST OSCILLATOR

This test oscillator is useful to ensure optimum operation of RF amplifier stages designed to work on the short-wave bands. Based on two crystal oscillators, it provides considerable output power (10 to 100 mW) to enable measuring intermodulation characteristics of high level and RF power stages. The quartz crystals used here not only serve as the frequency determining elements (2...20 MHz), but also as output filters to prevent one generated signal being lost in the other oscillator. With this in mind, tapped inductors L_1 and L_2 ensure freedom of mutual interference when the oscillator is used for frequencies higher than 10 MHz. Both inductors are wound as 12 turns of enamelled copper wire with a centre tap, on either a small balun or a suitably rated core with an air gap. Outputs of equal amplitude can be obtained by adjusting P_1.

The test oscillator consumes about 250 mA from a 60 V supply. This means that both transistors should be fitted with a heat-sink, and that chokes L_3 and L_4 should be capable of carrying about 150 mA. *B*





CORRECTIONS

Headphone amplifier

July/August 1987, Supplement p. 16
The Parts list should be amended as follows: R_6=2R7.

Synthesizer for SW receiver

July/August 1987, Supplement p. 61.
The mixer referred to in the 5th line of the text is not described in the Supplement of constructional projects, but forms part of a *Front end for SW receiver*, a project that will be included in *303 Circuits*, a forthcoming book from Elektor Electronics.

Toilet pointer

July/August 1987, Supplement p. 19
The 6th line of the text should read *proposed toilet pointer may be use—* .

Facsimile interface

April 1987, p. 43.
The listing for the BBC computer is wrong in serveral respects: the correct program is, therefore, given below.

Printed Resistors

June 1987, p. 36
The unit of resistivity is Ωmm²/m, not Ω/mm²/m.

Computerscope

September 1986, p. 62
Contrary to the correction given in the June 1987 issue, C_{15} is a 100p capacitor.

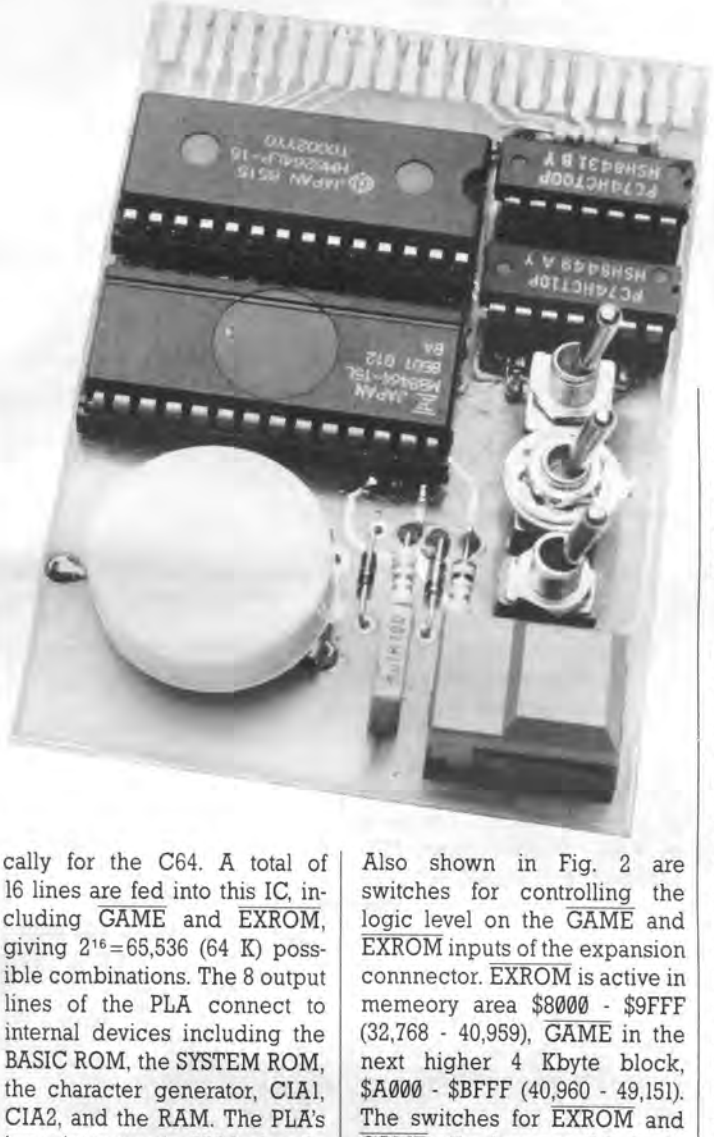
```
LIST
   10 *KEY0?&71=0:MRUN:M
   15 *KEY1?&71=1:MRUN:M
   20 *KEY10::M
   25 O=?&8F:IF O=&79 THEN GOTO 100
   30 VDU22,7:PRINT TAB(2,5)CHR$129"f0"CHR$135;
   31 PRINT"- start program in normal mode"TAB(2,7)CHR$129"f1"CHR$135;
   32 PRINT"- start program in inverse mode"TAB(2,13);
   33 PRINT" halt program with <BREAK>"TAB(25,20)"<RETURN>";
   34 REPEAT G=GET:UNTIL G=13:?&71=0:GOTO 100
   38
   40          (C) ELEKTOR 25 June 1987
   45
   50        connect pixelsync to CB1
   52        connect linesync to CB2
   53        connect pixelfax to PB0
   60
   70 Facsimile decoding routine for 1 & 2 Hz stations
   90
  100 DDRA = &FE63
  110 DDRB = &FE62
  120 PA   = &FE61
  130 PB   = &FE60
  140 ACR  = &FE6B
  150 PCR  = &FE6C
  160 INFR = &FE6D
  170 IER  = &FE6E
  180 BUFF = &FF00
  190
  200 MODE7:HIMEM=&7000
  205 REM  OR MODE 3
  206 REM  OR MODE 7 : HIMEM = &7000
  210 DIM MC% 600
  220 FOR O%=0 TO 2 STEP 2
  230 P%=MC%
  240 [
  245 OPT O%
  250 .begin   SEI
  260          LDA #&70  : STA &8F        \ clear printerbuffers
  270          LDA #&00  : STA &8E
  280          TAY
  290          LDX #&78
  300 .aa      STA (&8E),Y
  310          INY
  320          BNE aa
  330          INC &8F
  340          CPX &8F
  350          BNE aa
  370          STA point1+1               \ initialisation
  380          STA point2+1
  381          LDA #&70  : STA &73        \ default
  382          LDA #&74  : STA &74
  384          LDA #&74  : STA &75
  386          LDA #&78  : STA &76
  390\
  400          LDA #&00  : STA DDRB       \ PB all input
  410          LDA #&FF  : STA DDRA       \ PA all output , print
  420          LDA #&08  : STA PCR        \ CB2 IN_L independent , CB1 IN_L
  430                                     \ CA2 OUT handshake    , CA2 IN_L
  440          LDA #&03  : STA ACR        \ PB latch en. , PA latch en.
  450          LDA #&FF  : STA IER        \ BIT 7 set with INT
  460          LDA #&1B  : JSR print
  470          LDA #&41  : JSR print
  480          LDA #&08  : JSR print      \ Linefeed 8/72 inch
  495          LDA #&00  : STA &72        \ Status printer. bit 7 set as busy
  496\
  500          LDA #&1B  : STA &703C  : STA &743C
  510          LDA #&4C  : STA &703D  : STA &743D
  520          LDA #&C0  : STA &703E  : STA &743E \ double density
  530          LDA #&03  : STA &703F  : STA &743F \ 120 dots/in. for 960 bytes
  535\
  540 .swap    ASL &72
  550          BCC restr
  555          JMP err
  560 .restr   SEC
  570          ROR &72                       \ ready for printing
  580\
  590          LDA &73   : TAX  : LDA &74
  600          STA &73   : STA point1+2
  610          STX &74   : STX point2+2   \ swapped begin buffers
  620\
  630          LDA &75   : TAX  : LDA &76
  640          STA &75   : STX &76           \ swapped end buffers
  650\
  660          LDX #&40                      \ rotate ABS.X
  670          LDY #&3C                      \ print ABS.Y
  680          LDA #&0D  : STA PA            \ force CR to set CA1
  690          LDA #&08  : STA &70           \ ready for 8 lines
  695          LDA #&08  : STA INFR          \ clear CB2   linesync
  700\
  710 .waitnl LDA INFR
  720          AND #&08                \ mask CB2 , linesync
  730          BEQ waitnl
  740          LDA #&7D  : STA INFR  \ clear flags except CA1
  750\
  760 .fast    LDA INFR   : STA &80 : ROL A
  770          BCC fast
  780          LDA &80
  790          AND #&10                 \ mask CB1 pixel clock
  800          BNE pixel
  810          LDA &80    : AND #&02  \ mask printer ready
  820          BNE pbyte
  830          JMP fast
  840\
  850 .pixel   LDA PB     : EOR &71    \ inv/ninv byte
  860          LSR A
  870 .point1 ROL BUFF,X
  880          INX
  890          BNE fast
  900          INC point1+2                \ increment high byte pointer
  910          LDA point1+2 : CMP &75   \ end of buffer?
  920          BNE fast
  930          DEC &70    : BEQ swap     \ if 8 lines read
  940          LDA &73    : STA point1+2 \ else point to begin of buffer
  950          LDX #&40
  960          JMP waitnl
  970\
  980 .pbyte   ASL &72
  990          BCC fast                  \ not if status=0
 1000          ROR &72                  \ restore status
 1010 .point2 LDA BUFF,Y
 1020          STA PA                   \ print byte
 1030          INY
 1040          BNE fast
 1050          INC point2+2
 1060          LDA point2+2
 1070          CMP &76                  \ end of buffer?
 1080          BNE fast
 1090          ASL &72                  \ finished printing buffer: status=0
 1100          JMP fast
 1190\
 1200 .print   STA PA
 1210 .read    LDA INFR   : AND #&02  \ mask CA1 , printer ready
 1220          BEQ read
 1230          RTS
 1240
 1250 .err     CLI
 1260          BRK
 1270          EQUB &FF                 \ error number
 1280          EQUS "Printer overrun error"
 1284          EQUD &0D0A0A07
 1287          EQUS "Please press <BREAK>"
 1288          EQUD &0D0A0A0A
 1289          EQUS "Program halted"
 1290          EQUB &00                  \ close error string
 1300\
 1360 .end     CLI : RTS
 1400 ]
 1410 NEXT
 1420 PRINT''"Facsimile decoder for 1 & 2 Hz stations"
 1430 CALL begin
```

```
 735 USE THIS ROUTINE FOR 4 Hz STATIONS
 736 *********************************
 740 .reset  LDA #&7D  : STA INFR  \ clear flags except CA1
 750\
 760 .fast   LDA INFR  : AND #&10  \ mask CB1 pixel clock
 770         BEQ fast
 850 .pixel  LDA PB    : EOR &71   \ inv/ninv byte
 860         LSR A
 870 .point1 ROL BUFF,X
 880         INX
 890         BNE fast
 900         INC point1+2              \ increment high byte pointer
 910         LDA point1+2 : CMP &75   \ end of buffer?
 920         BNE fast
 930         DEC &70   : BEQ swap     \ if 8 lines read
 940         LDA &73   : STA point1+2 \ else point to begin of buffer
 950         LDX #&40                 \ and restore X to &40
 960 .pbyte  LDA INFR  : STA &80 : AND #&08 \ mask NL
 965         BNE reset
 970         LDA &80   : AND #&02              \ mask printer ready
 975         BEQ pbyte
 980         ASL &72
```

16 KBYTE CMOS RAM FOR C64

by P Verhoosel

A non-volatile block of RAM or pseudo-ROM for plugging into the Commodore 64's expansion slot.



The expansion port at the rear of the Commodore 64 microcomputer is a 44-pin (22+22) female edge connector. The expansion slot—also referred to as bus, cartridge or module port—enables plugging in extension modules that require direct access to the address bus, data bus, and a number of control lines, of the Type 6510 CPU and its support chips inside the computer. Because of this direct connection, due care should be taken not to damage the system by inappropriate connections, overloads, or short-circuits. The signal functions and pin assignment of the expansion port are shown in Table 1 and Fig. 1 respectively. Viewed from the computer's keyboard, and counting from the left to the right, pins 1-22 inclusive form the upper row, and pins A-Z inclusive the lower row. Notice that letters G, I, O and Q are not used. Connections $\overline{\text{GAME}}$ and $\overline{\text{EXROM}}$ make it possible to gain external control over the C64's memory configuration, and have special significance for the present memory module.

The system configuration

At the heart of the C64's memory decoding circuitry is integrated circuit U_{17}, a Programmable Logic Controller (PLA), manufactured specifically for the C64. A total of 16 lines are fed into this IC, including $\overline{\text{GAME}}$ and $\overline{\text{EXROM}}$, giving $2^{16}=65{,}536$ (64 K) possible combinations. The 8 output lines of the PLA connect to internal devices including the BASIC ROM, the SYSTEM ROM, the character generator, CIA1, CIA2, and the RAM. The PLA's input/output ratio, 256:1, already indicates that a number of input combinations are necessarily duplicate and/or illegal to give a useful configuration of the C64' memory map, which is shown schematically in Fig. 2. The decimal and hexadecimal address notations are given to the left and the right of the 4 Kbyte memory blocks, respectively. When the C64 powers up with the original operation system, the following PLA inputs are driven logic high: $\overline{\text{LORAM}}$, $\overline{\text{HIRAM}}$, $\overline{\text{EXROM}}$, $\overline{\text{GAME}}$, $\overline{\text{CHAREN}}$.

Also shown in Fig. 2 are switches for controlling the logic level on the $\overline{\text{GAME}}$ and $\overline{\text{EXROM}}$ inputs of the expansion connnector. $\overline{\text{EXROM}}$ is active in memeory area \$8000 - \$9FFF (32,768 - 40,959), $\overline{\text{GAME}}$ in the next higher 4 Kbyte block, \$A000 - \$BFFF (40,960 - 49,151). The switches for $\overline{\text{EXROM}}$ and $\overline{\text{GAME}}$ offer four possible logic configurations:

a) $\overline{\text{GAME}}$ = 1; $\overline{\text{EXROM}}$ = 1.
b) $\overline{\text{GAME}}$ = 0; $\overline{\text{EXROM}}$ = 1
c) $\overline{\text{GAME}}$ = 1; $\overline{\text{EXROM}}$ = 0
d) $\overline{\text{GAME}}$ = 0; $\overline{\text{EXROM}}$ = 0

Although not harmful to the C64 hardware, combination **b** produces a hang-up, which can only be ended by altering the switch configuration and resetting the computer.

Combination **a** is valid when the computer is powered up, while **c** can be selected with the aid of switch S_2 on the present board. An additional switch, S_3, can be closed following S_2, and enables selecting combination **d**. Combination **b** is impossible to select thanks to the practical switch configuration.

Circuit description

The circuit diagram of the RAM extension is shown in Fig. 3. When S_3 is opened, the RAM module is switched to the write protect mode, and resistor R_1 ensures a fixed level at the $\overline{\text{WE}}$ (write enable) inputs of RAM chips IC_3 and IC_4, which then behave as ROMs, since they can only be read from, not written to. Gates N_3 and N_5-N_7 combine address lines A13, A14 and A15 into a $\overline{\text{CS}}$ (chip select) line for each of the 8 Kbyte RAMs. Gate N_1 plus switches S_{2a} and S_{3a} ensure the correct set-up times for read operations in the RAMs. Parallel combination R_3-D_1 charges the on-board 3.6 V NiCd battery from the computer's 5 V supply. When the computer is off, the battery supplies the (very low) data retention current for the CMOS RAM chips. Components C_1-R_2-D_2 prevent dips and transients on the RAM supply lines when the computer is switched off, and the battery takes over. It should be noted that a dry battery is preferable over a NiCd cell when the computer is not used for periods longer than about a month, because a NiCd cell inevitably loses its charge due to its self discharge current. R_1 is omitted when a dry battery is used.

Applications

Switched to configuration **c**, the battery back-up RAM makes it possible to slightly modify the resident BASIC interpreter for individual purposes, copy parts of it into the RAM/ROM module, develop and store new utilities, or have machine language programs permanently available. Memory area 32,768 to 40,959 is covered entirely by IC_3, and is fully accessible to the programmer.

Configuration **d** selects the full 16 KByte RAM block, which then takes the place of the 8 KByte Microsoft BASIC ROM and the internal memory block in this area. When RESET switch S_4 is pressed, the operating system in the C64 searches for the following tokenized code starting at $8004:

$8004	$8005	$8006	$8007	$8008
C3	C2	CD	38	30

Translated into ASCII, this stands for *CBM80* if the MSB, D7, is ignored. If this 5-byte string is found (cold boot), the CPU jumps to the address stored in location $8000 (L) and $8001 (H). The 16-bit vector for a warm start is located in the next two higher locations, $8002 and $8003.

Construction

The compact, ready-made printed circuit board for constructing the RAM extension is a double-sided, but not through-plated, type, which holds all the components—inclusive of the battery and the switches—and plugs straight into the C64's expansion slot. The track layouts and component mounting plan are given in Fig. 4. Commence the construction with fitting the resistors, capacitors, diodes and the wire link. Note that some components, including the IC sockets, are soldered at both sides of the PCB to effect through-plating. At the copper side, all connections are soldered, at the component side only those whose solder islands are not covered by the component overlay. The 2 holes in between S_3 and IC_2 are through-plated with the aid of component wire. The miniature switches can be fitted direct onto the board with the aid of bits of left over component leads. RESET key S_4 is a Type Digitast from ITT/Schadow, and should not present problems as to mounting. The 3.6 V NiCd battery should be fitted securely to make for a compact and sturdy extension module. Finally, plug in the integrated circuits, and the back-up memory is ready for use.

Note: Always switch off the computer before inserting or removing the 16 Kbyte RAM module. *St*

1

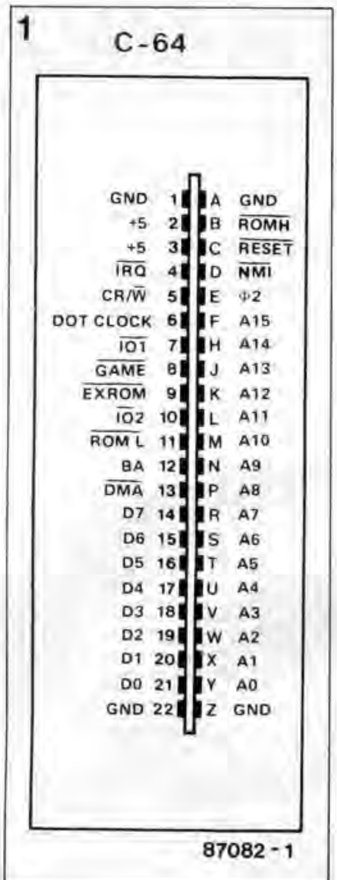


Fig. 1. Pin assignment on the expansion port at the rear of the C64 computer.

Table 1 Signal functions on the C64 expansion port:

Pin	Signal	Function
1 22 Z	GND	System ground
2/3	+5 V (V_{cc})	Power supply for User Port and Cartridge devices (450 mA max.)
4	$\overline{IRQ}$	Maskable CPU interrupt request line (active low).
5	R/$\overline{W}$	CPU output line. Memory read: 1; memory write: 0.
6	DOT CLOCK	8.18 MHz dot clock signal from video controller.
7 11 B 10	$\overline{I/O1}$ $\overline{ROML}$ $\overline{ROMH}$ $\overline{I/O2}$	Active low outputs for memory control.
8 9	$\overline{GAME}$ $\overline{EXROM}$	Active low inputs for memory control.
12	BA	Bus available signal from the VIC-11 controller.
13	$\overline{DMA}$	Direct memory access request line.
14 : : 21	D7 : : D0	Unbuffered 6510 databus.
C	$\overline{RESET}$	Direct CPU reset line for initialising the computer.
D	$\overline{NMI}$	Non-maskable CPU interrupt line.
E	Φ2	CPU clock signal.
F : : Y	A15 : : A0	Unbuffered address lines.

2

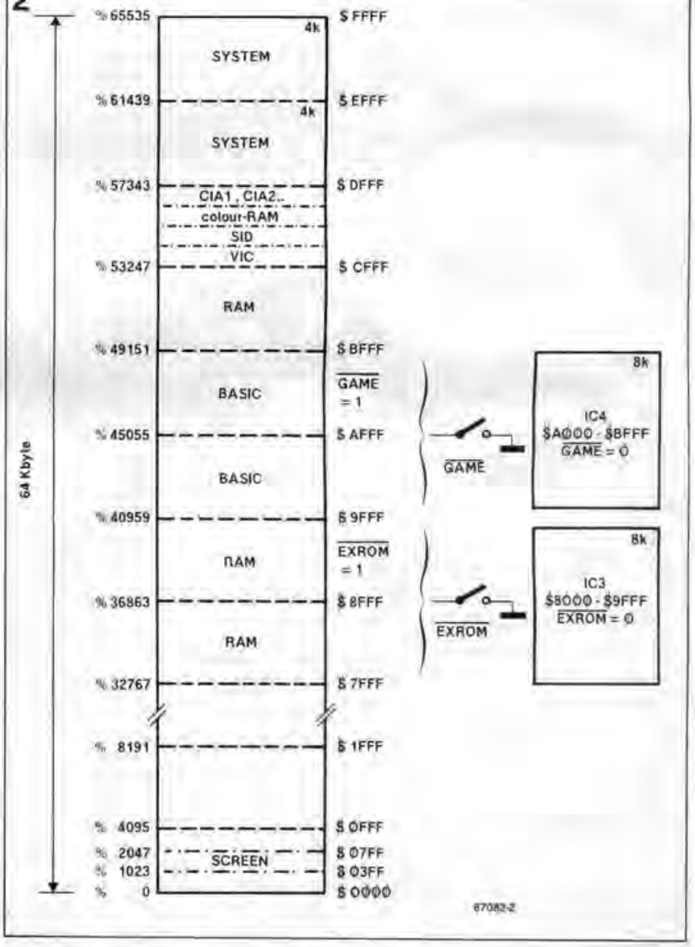


Fig. 2. Essentials of the C64's memory map.

3

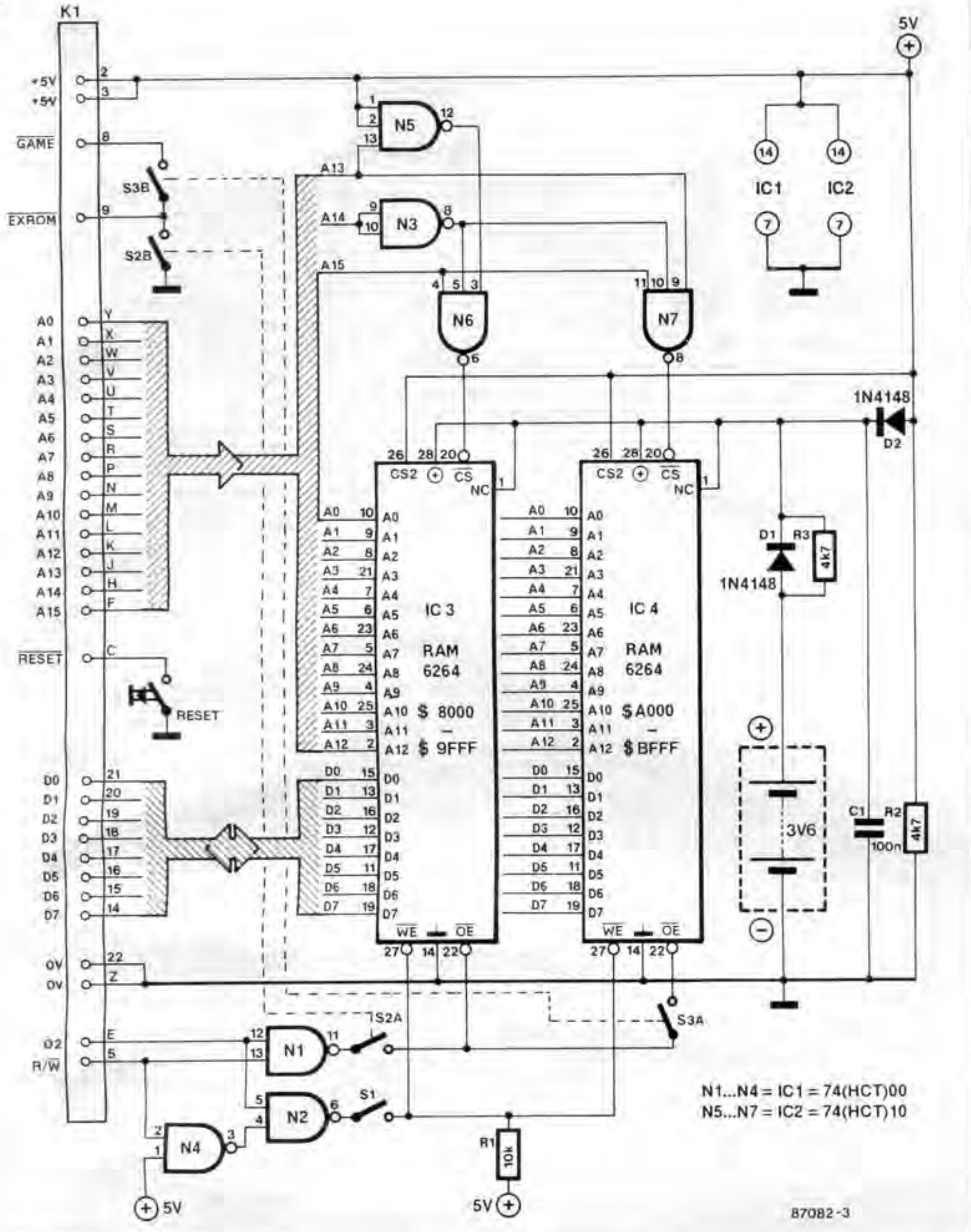


Fig. 3. Circuit diagram of the non-volatile 16 Kbyte RAM module.

Parts list

Resistors (±5%):
R_1 = 10K
R_2;R_3 = 4K7

Capacitor:
C_1 = 100n

Semiconductors:
D_1;D_2 = 1N4148
IC_1 = 74HCT00
IC_2 = 74HCT10
IC_3;IC_4 = 6264 8K x 8 static CMOS RAM

Miscellaneous:
S_1 = miniature SPST switch.
S_2;S_3 = miniature DPDT switch.
S_4 = Digitast momentary action key, Electromail stock no. 337-368.
PCB mount sealed 3.6 V NiCd battery with solder tags, e.g. Maplin order no. RK46A.
PCB Type 87082 (available through the Readers services).

Fig. 4. The printed circuit board for making the RAM module.

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